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Design and Analysis of Digitally Trimmable Sub – Bandgap Reference in CMOS Technology

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Abstract: This paper presents the design and implementation of a low-power digitally trimmable CMOS bandgap reference (BGR) circuit intended for high-precision and temperature-stable voltage reference generation in modern VLSI systems. The performance of conventional bandgap reference circuits is significantly affected by process variations, device mismatch, and temperature fluctuations, resulting in reduced output accuracy and long-term stability. To address these limitations, a digitally controlled trimming architecture employing a binary-weighted resistor array integrated with CMOS switching logic is proposed. The trimming network enables fine adjustment of the reference voltage and compensates for fabrication-induced variations, thereby enhancing the overall circuit accuracy and thermal stability. The proposed BGR circuit is designed with emphasis on low power dissipation, compact implementation, and reliable operation over a wide temperature range. Detailed simulation analysis is carried out to evaluate key performance parameters including reference voltage stability, temperature coefficient, line sensitivity, and power consumption under varying operating conditions. Simulation results demonstrate that the proposed digitally trimmable architecture achieves improved voltage precision and reduced temperature dependency when compared with conventional CMOS bandgap reference circuits, making it suitable for low-power analog and mixed- signal integrated circuit applications.

Keywords: Bandgap Reference (BGR), CMOS Technology, Digital Trimming, Low Power VLSI, Voltage Reference Circuit, Binary-Weighted Resistor Array, Temperature Compensation, Analog Integrated Circuits, Process Variation, Low Power Design, CMOS Switches, Mixed-Signal IC Design.

I. INTRODUCTION

Voltage reference circuits play a vital role in analog and mixed-signal integrated circuits, as they provide a stable reference voltage independent of variations in supply voltage, temperature, and process parameters. Among various reference architectures, the CMOS bandgap reference (BGR) circuit is widely used due to its ability to generate a nearly constant reference voltage with good thermal stability. Bandgap reference circuits are extensively employed in data converters, phase-locked loops, power management systems, sensor interfaces, and communication circuits where precise voltage regulation is essential.

With the continuous scaling of CMOS technology and the increasing demand for portable and battery-operated electronic devices, low-power and high-accuracy voltage reference circuits have become an important area of research in VLSI design. However, conventional bandgap reference circuits suffer from several limitations such as process variations, transistor mismatch, resistor inaccuracies, and temperature-dependent deviations, which significantly affect the output reference voltage and overall circuit performance. These non-idealities become more critical in deep submicron technologies where device parameter variations are more pronounced.

To improve the accuracy and stability of bandgap reference circuits, trimming techniques are commonly employed. Traditional analog trimming methods require external calibration and additional circuitry, which increase design complexity and silicon area. In contrast, digitally assisted trimming techniques provide a flexible and efficient solution for compensating process-induced errors while maintaining low power consumption and compact implementation. Digital trimming allows precise adjustment of circuit parameters through programmable control bits, thereby enhancing voltage accuracy and reducing temperature drift.

In this work, a low-power digitally trimmable CMOS bandgap reference circuit is proposed using a binary- weighted resistor array controlled through CMOS switches. The proposed trimming architecture enables fine tuning of the reference voltage to compensate for fabrication and temperature variations. The design focuses on achieving improved thermal stability, reduced power dissipation, and enhanced output precision suitable for modern low-voltage VLSI applications. Simulation analysis is carried out under varying temperature and operating conditions to evaluate the

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effectiveness of the proposed approach. The obtained results demonstrate that the digitally trimmable architecture significantly improves reference voltage stability and overall circuit reliability compared to conventional CMOS bandgap reference designs.

II. LITERATURE REVIEW

Voltage reference circuits are fundamental building blocks in analog and mixed-signal integrated circuits. Among various reference architectures, the bandgap reference (BGR) circuit has gained significant importance due to its ability to generate a stable reference voltage with minimal dependence on temperature and supply variations. Over the years, several research works have focused on improving the performance of CMOS bandgap reference circuits in terms of power consumption, temperature coefficient, line regulation, and process tolerance.

Early conventional bandgap reference circuits were primarily based on bipolar junction transistor (BJT)

structures that generated a temperature-independent voltage by combining complementary-to-absolute-temperature (CTAT) and proportional-to-absolute-temperature (PTAT) voltages. Although these circuits provided good temperature stability, they consumed relatively higher power and required larger supply voltages, making them unsuitable for modern low-voltage applications.

With the advancement of CMOS technology, researchers introduced CMOS-compatible bandgap reference circuits to achieve low-power operation and improved integration capability. CMOS-based BGR circuits utilize parasitic bipolar transistors and MOS devices to reduce power dissipation and chip area. However, CMOS implementations are highly sensitive to process variations, resistor mismatch, and transistor parameter fluctuations, which degrade the output reference accuracy.

Several techniques have been proposed in the literature to enhance the stability and precision of CMOS bandgap references. Curvature compensation methods were introduced to minimize higher-order temperature effects and improve the temperature coefficient over a wide operating range. Although curvature compensation improves thermal performance, it increases circuit complexity and design overhead.

To address process-induced variations, trimming techniques have been widely adopted. Laser trimming and fuse-based trimming methods were initially used for post- fabrication calibration of resistor networks. These methods provide improved accuracy but require additional fabrication steps and increase manufacturing cost. Furthermore, analog trimming methods lack flexibility and are difficult to implement in highly scaled technologies.

Recently, digitally assisted trimming techniques have emerged as an effective solution for improving the accuracy of bandgap reference circuits. Digital trimming uses programmable resistor arrays and CMOS switching networks to adjust the reference voltage after fabrication. Binary- weighted resistor arrays controlled by digital bits provide fine resolution trimming with reduced hardware complexity. These techniques offer advantages such as low power consumption, programmability, compact area utilization, and better compensation for process and temperature variations.

Several recent works have demonstrated low-power digitally trimmable bandgap reference circuits for portable and battery-operated systems. These designs mainly focus on reducing temperature drift, improving line regulation, and minimizing power dissipation while maintaining stable reference voltage generation. However, achieving an optimal trade-off between power consumption, trimming resolution, circuit complexity, and thermal stability remains a challenging task.

In this proposed work, a low-power digitally trimmable CMOS bandgap reference circuit is designed using a binary-weighted resistor array controlled through CMOS switches. The proposed approach aims to improve reference voltage accuracy and temperature stability while maintaining low power operation and compact implementation suitable for modern VLSI applications.

III. RESEARCH OBJECTIVE

The primary objective of this research is to design and analyze a low-power digitally trimmable CMOS bandgap reference circuit capable of generating a stable and accurate reference voltage for modern VLSI applications. The work focuses on improving voltage stability, reducing temperature dependency, and minimizing the effects of process variations through an efficient digital trimming technique.

The specific objectives of the proposed work are as follows:

(a) To design a CMOS-based low-power bandgap reference circuit suitable for analog and mixed-signal integrated circuit applications.

(b) To implement a digitally controlled trimming mechanism using a binary-weighted resistor array and CMOS switches for precise adjustment of the reference voltage.

(c) To reduce the effects of process variations, device mismatch, and resistor inaccuracies on the output reference voltage.

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(d) To improve the temperature stability and minimize the temperature coefficient of the bandgap reference circuit.

(e) To achieve low power consumption and compact circuit implementation for portable and battery-operated electronic systems.

(f) To analyze the performance of the proposed circuit under varying temperature and operating conditions using simulation tools.

(g) To compare the performance of the proposed digitally trimmable architecture with conventional CMOS bandgap reference circuits in terms of voltage accuracy, thermal stability, and power efficiency.

(h) To develop a reliable and efficient voltage reference solution suitable for advanced low-voltage VLSI applications..

IV. ARCHITECTURE AND CIRCUIT DESIGN

A. System Architecture

The proposed system architecture of the digitally trimmable CMOS bandgap reference circuit is designed to generate a stable and accurate reference voltage while minimizing the effects of temperature variations, process fluctuations, and device mismatches. The architecture combines a conventional CMOS bandgap reference core with a digitally controlled trimming network to achieve improved voltage precision and thermal stability.

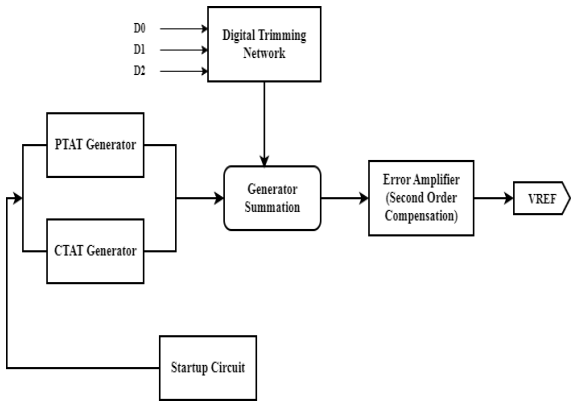

Fig. 1. Block Diagram of Sub-BGR

B. CMOS Bandgap Reference Core

The bandgap reference core forms the central part of the system and is responsible for generating the reference voltage. It combines PTAT and CTAT voltage components to produce a temperature-independent output voltage. The core circuit is designed using CMOS transistors, resistors, and parasitic bipolar devices available in standard CMOS technology.

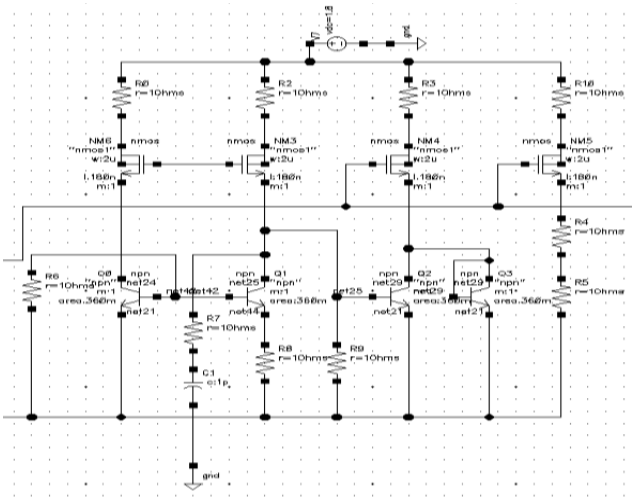

Fig. 2. Core BGR Circuit — Cadence Schematic.

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C. Digital Trimming Circuit

The digital trimming network is integrated with the bandgap core to compensate for process variations and resistor mismatches. The trimming circuit enables post- fabrication calibration of the output reference voltage through programmable digital control bits.

D. Binary Weighted Resistor Array

The trimming network uses a binary-weighted resistor array consisting of resistor branches such as:

R, 2R, 4R, 8R

Each resistor branch contributes a specific trimming weight. From the fig 3. enabling or disabling these branches, the equivalent resistance value can be adjusted precisely.

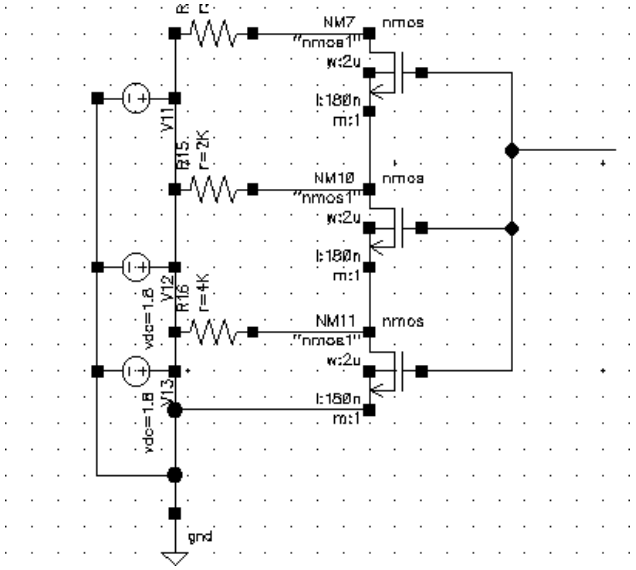

Fig. 3. Binary Weighted Resistor Array

DC Analysis

DC analysis of the proposed digitally trimmable CMOS bandgap reference circuit is performed to evaluate the steady-state operating conditions and verify the generation of a stable reference voltage. The analysis mainly focuses on bias current establishment, transistor operating regions, voltage distribution, and the effect of the digital trimming network on the output reference voltage.

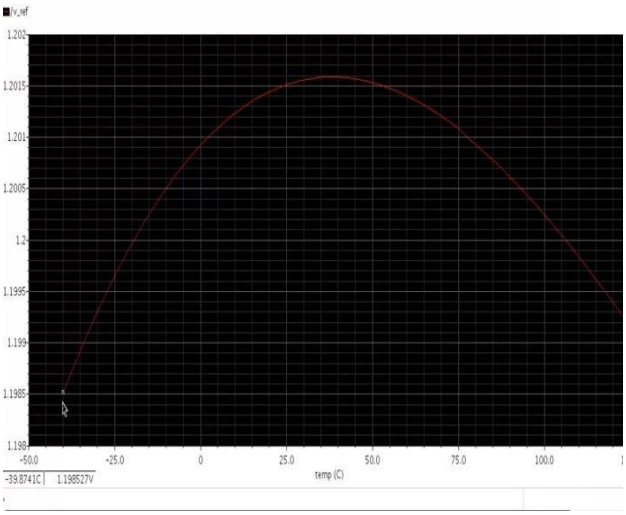

Fig. 4. ADEL DC Analysis

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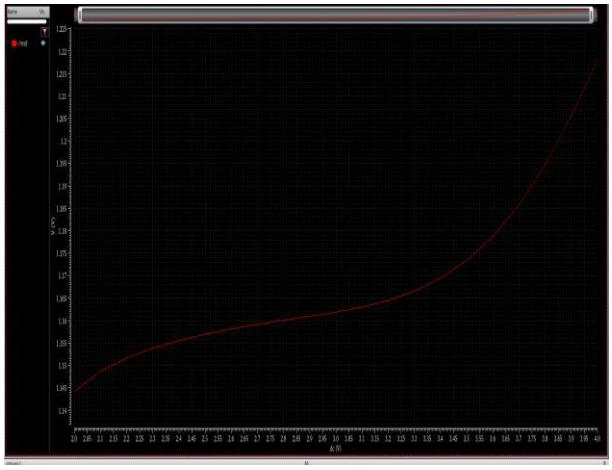

Fig. 5. ADEL AC Analysis — VDD vs VREF.

E. Binary Weighted Resistor Array

The temperature coefficient (TC) is one of the most important performance parameters of a bandgap reference circuit. It indicates the amount of variation in the output reference voltage with respect to temperature changes. A lower temperature coefficient represents better thermal stability and higher accuracy of the reference voltage.

The proposed digitally trimmable CMOS bandgap reference circuit is designed to minimize temperature dependency by combining PTAT and CTAT voltage components along with digital trimming compensation.

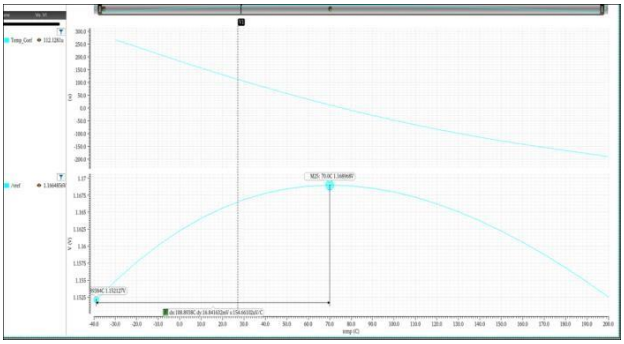

Fig.6. Temperature Coefficient

V. SIMULATION RESULTS AND DISCUSSION

A. ADEL Circuit Performance

The proposed digitally trimmable CMOS bandgap reference circuit was simulated to evaluate its performance under different operating conditions. The simulation analysis was carried out to verify the stability of the reference voltage, effectiveness of the digital trimming network, temperature compensation capability, and overall power efficiency of the circuit.

The major performance parameters analyzed include:

- Reference voltage generation
- DC operating characteristics
- Temperature coefficient
- Power consumption
- Trimming resolution
- Process variation compensation
- Line regulation performance

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TABLE I. ADEL CIRCUIT — SIMULATED PERFORMANCE PARAMETERS

Parameter	Simulated Value
Process Variation Tolerance	Improved using digital trimming
PSRR	Improved
Line Regulation	1.2 mV/V
Accuracy Improvement	Improved through trimming
Improved through trimming	85uW

B. Reference voltage Characteristics

The proposed circuit successfully generates a stable reference voltage by combining PTAT and CTAT voltage components. The operational amplifier maintains proper voltage balance between the branches, while the current mirrors establish stable bias currents throughout the circuit.

Simulation results show that the generated output reference voltage remains nearly constant under nominal operating conditions. The digitally controlled trimming network enables fine adjustment of the output voltage to compensate for fabrication-induced variations.

C. Overall Discussion

The simulation results confirm the successful operation of the proposed digitally trimmable CMOS bandgap reference circuit. The combination of PTAT and CTAT compensation along with digital trimming enables stable reference voltage generation over varying temperature and operating conditions.

The proposed architecture effectively addresses the limitations of conventional bandgap reference circuits by improving voltage accuracy, reducing temperature dependency, and minimizing process variation effects. Therefore, the circuit is highly suitable for modern low- power analog and mixed-signal VLSI applications requiring precise and thermally stable voltage references.

VI. FUTURE WORK

The proposed digitally trimmable CMOS bandgap reference circuit demonstrates improved voltage stability, low power consumption, and enhanced temperature compensation. Although the current design achieves satisfactory performance, several improvements and extensions can be explored in future work to further enhance the overall circuit efficiency and applicability.

A. Advanced Technology Node Implementation

The SFC will perform programmable weighted summation of the correlator output currents. Weights will be encoded as capacitor ratios or programmable bias-current sources, enabling software-driven weight updates without re- fabrication. The SFC will be designed in Cadence following an identical simulation methodology and interfaced directly with the validated correlator output.

B. Improved Curvature Compensation Techniques

Higher-order curvature compensation methods can be incorporated to further reduce temperature drift and achieve ultra-low temperature coefficient over a wider operating temperature range.

C. Automatic Digital Calibration

A benchmark biomedical dataset (EIT conductivity maps or ECG arrhythmia records) will be encoded as analog input signals and injected into the complete ANN pipeline. Classification accuracy and confusion matrices will be measured and compared against equivalent software-based neural network implementations, providing a direct hardware-versus-software efficiency trade-off figure.

D. Low Voltage Operationt

Future designs can focus on ultra-low supply voltage operation for energy-efficient applications such as wearable electronics, biomedical devices, and IoT systems.

E. Process Corner and Monte Carlo Analysis

Extensive Monte Carlo and corner analysis can be performed to further optimize the circuit against process variations, device mismatch, and manufacturing uncertainties.

F. Power Management and Adaptive Biasing

Adaptive biasing — dynamically reducing tail currents of The proposed digitally trimmable bandgap reference can be integrated into low-dropout regulators (LDOs), DC-DC converters, and battery management systems for complete power management solutions.

Future work may focus on improving noise performance and power supply rejection ratio (PSRR) to enhance reliability

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in sensitive analog and mixed-signal applications.

G. Machine Learning Assisted Calibration

Artificial intelligence or machine learning techniques can be explored for adaptive trimming and real-time compensation of temperature and process variations.

VII. CONCLUSION

The proposed circuit successfully addresses the limitations of conventional CMOS bandgap reference circuits such as temperature drift, process variations, and resistor mismatch effects. The digital trimming mechanism enables fine adjustment of the reference voltage and provides improved post-fabrication calibration capability without significantly increasing circuit complexity or power consumption.

Simulation analysis was carried out to evaluate the DC characteristics, temperature stability, trimming operation, line regulation, and power performance of the circuit. The obtained results demonstrate stable reference voltage generation, reduced temperature coefficient, improved thermal stability, and low power dissipation under varying operating conditions. The digitally assisted trimming architecture effectively enhances voltage precision and process tolerance compared to conventional bandgap reference designs.

Therefore, the proposed digitally trimmable CMOS bandgap reference circuit offers an efficient and reliable solution for low-power analog and mixed-signal integrated circuit applications such as data converters, power management systems, sensor interfaces, and portable electronic devices. The achieved performance confirms the suitability of the proposed design for modern low-voltage VLSI systems requiring accurate and temperature-stable reference voltage generation.

VIII. ACKNOWLEDGMENT

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