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DESIGN OF A MIXED SIGNAL VCO BASED ADC FOR HIGH SPEED APPLICATIONS

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Abstract: This paper demonstrates a power-efficient implementation of a mixed-signal Analog-to-Digital Converter (ADC) based on a Voltage-Controlled Oscillator (VCO). Conventional Flash ADCs face significant limitations in power and area at multi-GS/s speeds as comparator counts grow exponentially. The proposed hybrid Flash-VCO architecture overcomes these challenges by shifting fine quantization into the time domain. A current-starved ring oscillator scheme is employed for the VCO to achieve high efficiency and CMOS scalability. Simulation results confirm that this approach reduces power consumption and mismatch sensitivity, making it suitable for high-speed, low-resolution biomedical and wireless applications.

Keywords: Voltage-Controlled Oscillator (VCO), Flash ADC, Mixed-Signal Design, Current-Starved Oscillator, Time-Domain Quantization.

I. INTRODUCTION

A VCO-based mixed-signal Flash ADC combines the ultra-high speed of Flash architectures with time-domain signal processing for improved efficiency. In this approach, the analog input is converted into a frequency-modulated signal using a VCO, followed by fast parallel quantization. This architecture reduces power consumption and mismatch sensitivity, making it highly suitable for deep-submicron CMOS nodes where time resolution is superior to voltage headroom.

II. PROBLEM STATEMENT AND OBJECTIVE

Flash-only ADCs hit limits in power and area at multi-GS/s speeds because comparator count grows exponentially. Flash-VCO hybrid based ADCs help to overcome these limits by shifting fine quantization into the time domain. This methodology scales well with CMOS technology, supports low-voltage operation, and is more robust to device mismatch compared to conventional voltage-domain processing.

III. SYSTEM ARCHITECTURE

A. Voltage to Frequency Converter

The Voltage to Frequency Converter (VFC) uses a Current-Starved Ring Oscillator as its analog core. The oscillation frequency is linearly proportional to the input control voltage. By controlling the amount of current available to charge or discharge the capacitive load of each inverter stage, the delay—and thus the frequency—is modulated by the analog input signal.

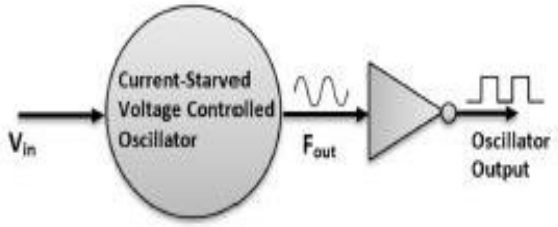

Fig. 1 voltage to frequency converter

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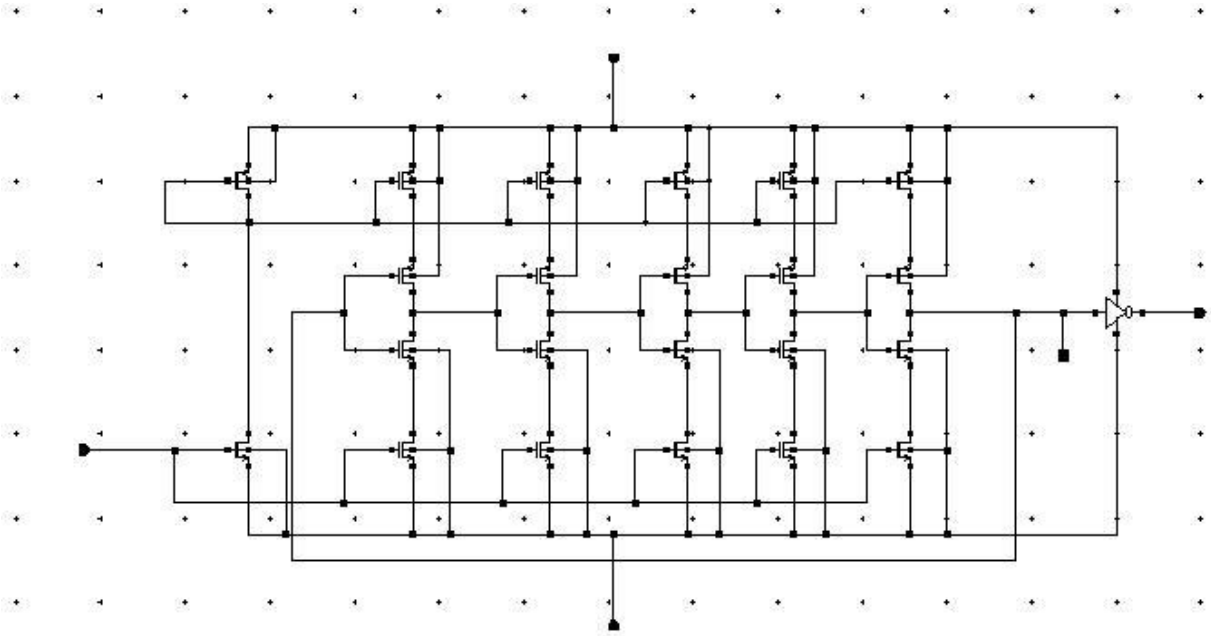

Fig. 2 schematic of voltage to frequency converter

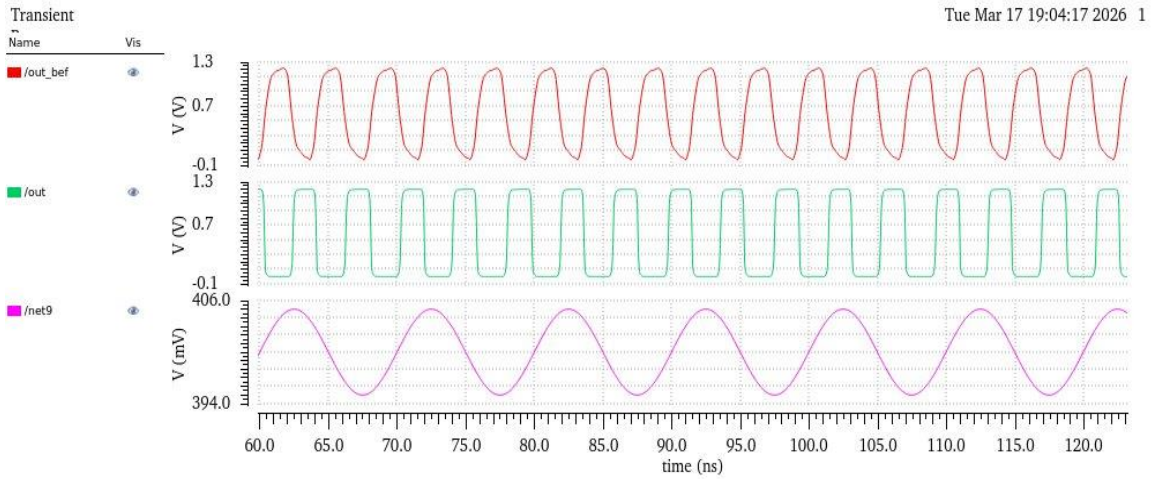

Fig. 3 Transient Response of voltage to frequency converter

B. Frequency to Digital Converter

The Frequency to Digital Converter (FDC) utilizes a reset counter to transform the frequency-modulated pulses generated by the VCO into a digital code. During each sampling interval, the rising edges of the VFC output are counted. This captured count represents the VCO frequency and, consequently, the sampled analog input voltage.

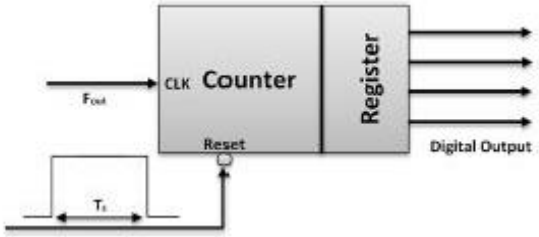

Fig. 4 Frequency to digital converter

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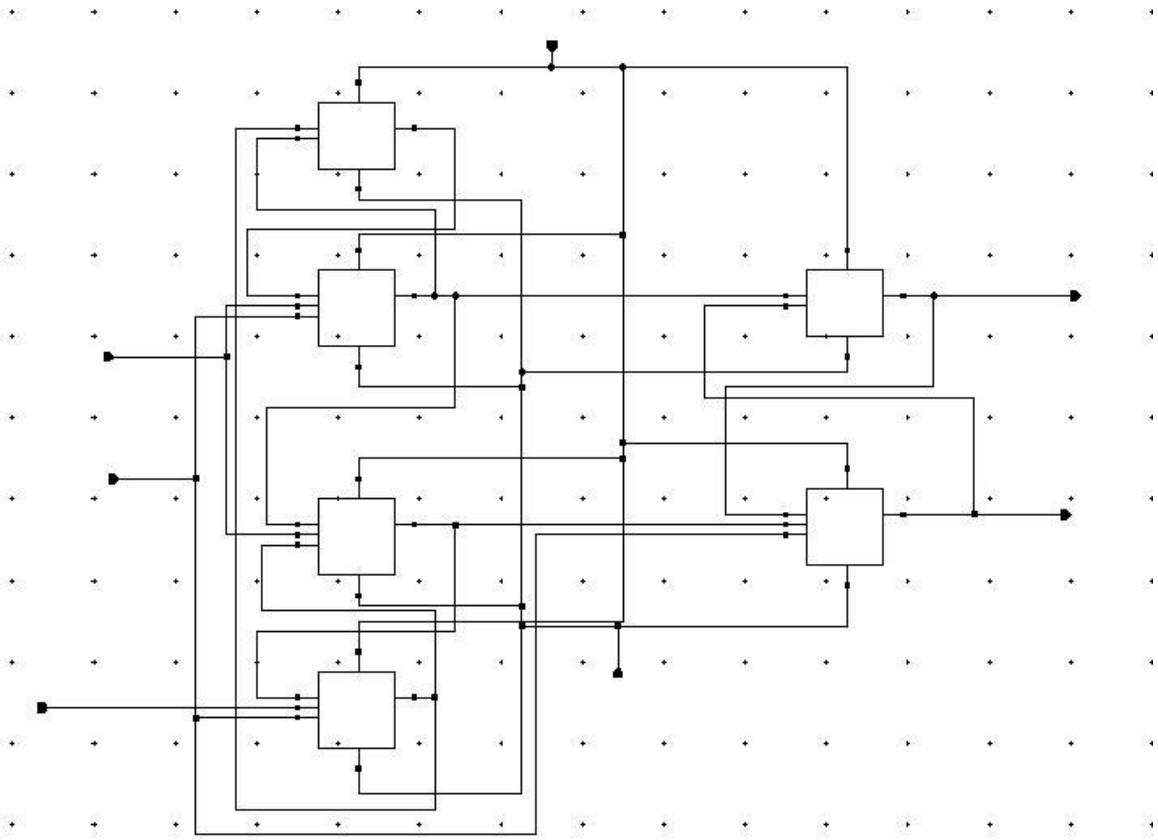

Fig. 5 D-Flipflop

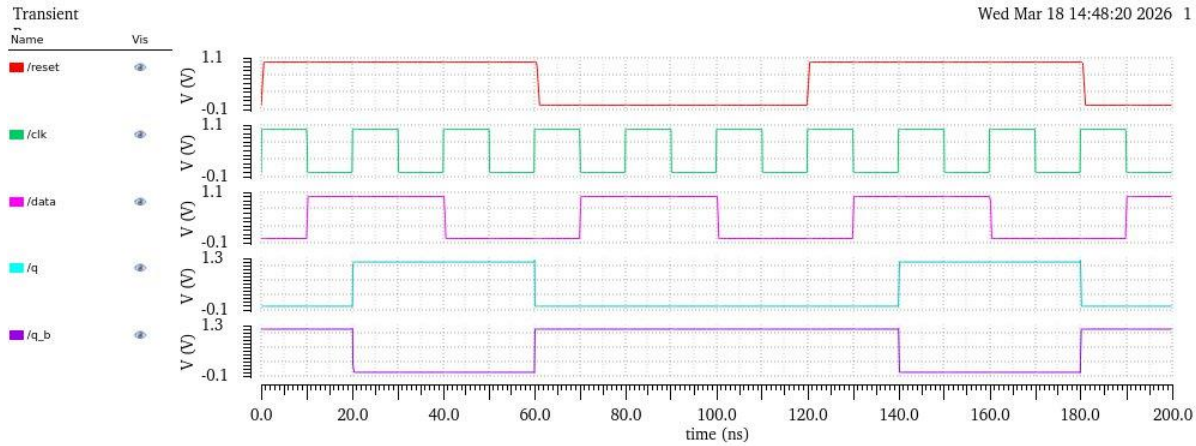

Fig. 6 Transient response of D-Flipflop

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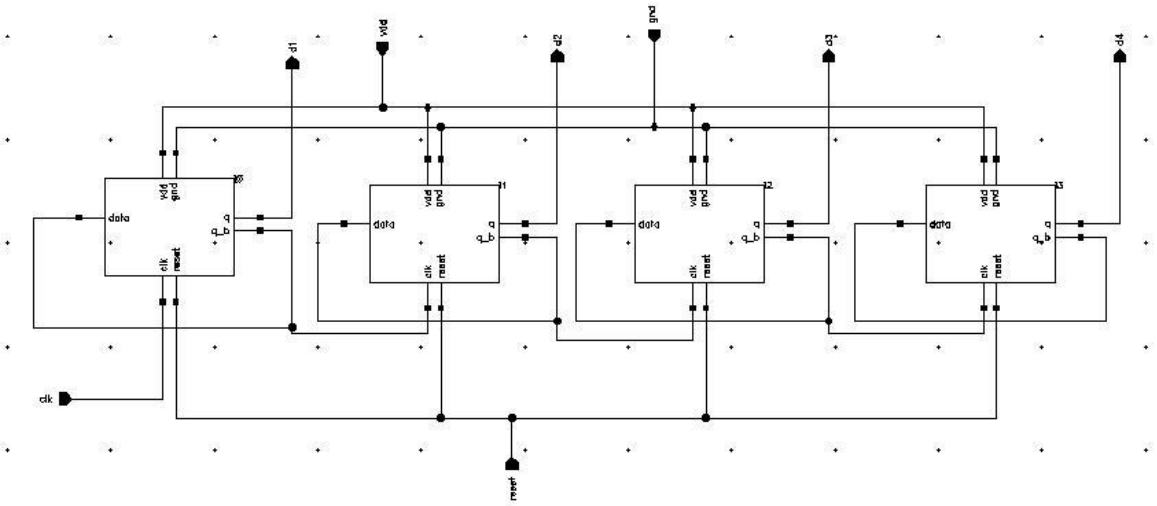

Fig. 7 Schematic of Reset counter

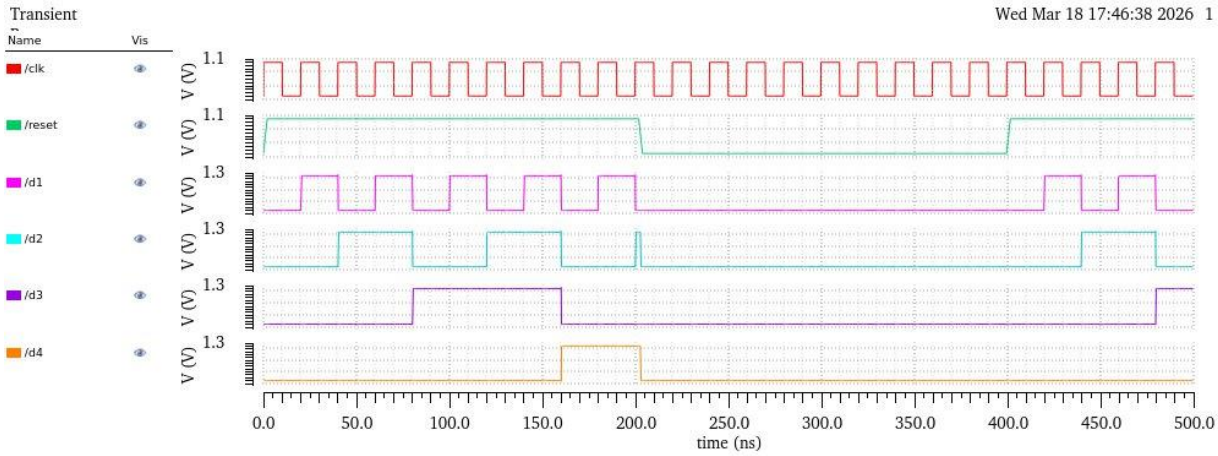

Fig. 8 Transient Response of Reset counter

IV. HARDWARE IMPLEMENTATION

The proposed architecture is implemented using 130 nm CMOS technology. Key components such as the Sense-Amplifier Flip-Flops (SAFF), multi-phase ring oscillators, and NAND-based D-Flip Flops were designed for high-speed operation. The VCO behavior was modeled using Verilog-A, while the current-starved ring oscillator was implemented at the transistor level for precise power and timing analysis.

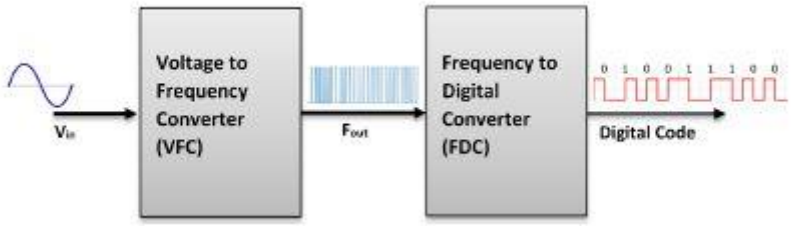

Fig. 9 Block Diagram of proposed VCO based ADC

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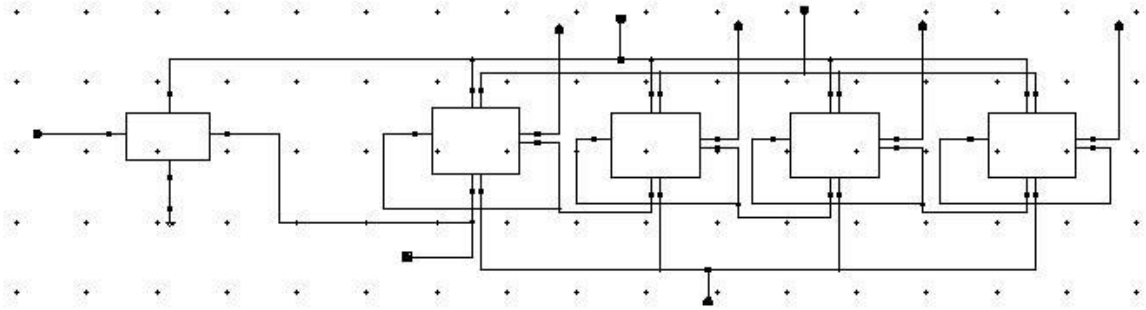

Fig. 10 Schematic of proposed VCO based ADC

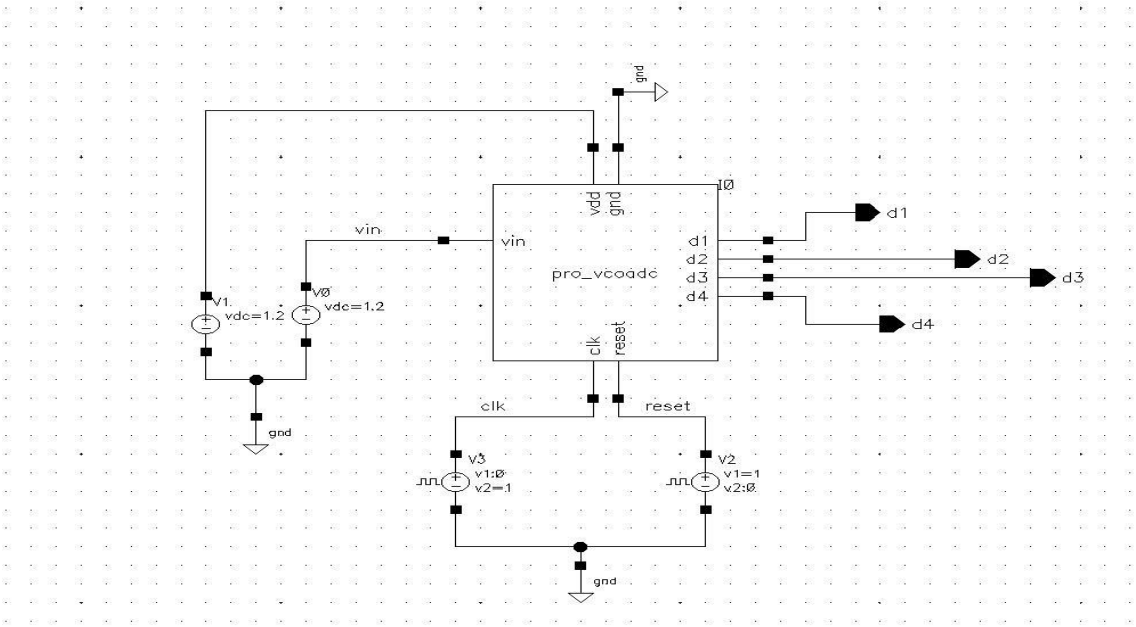

Fig. 11 Test Bench of proposed VCO based ADC

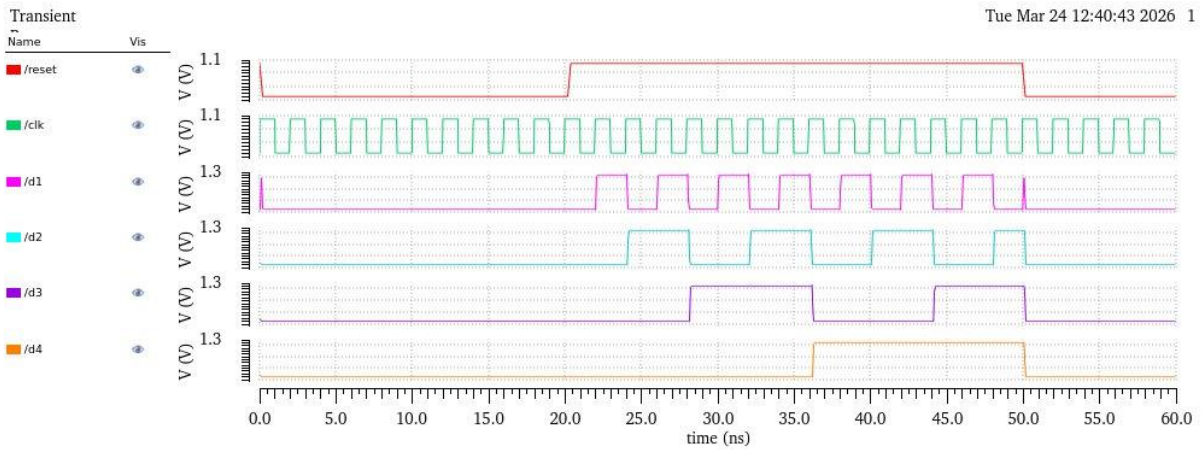

Fig. 12 Transient Response of proposed VCO based ADC

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V. CONCLUSION

This paper presented a mixed-signal hybrid ADC architecture combining Flash and VCO-based quantization. The design effectively bridges the gap between analog inputs and digital processing by leveraging time-domain signal processing. The current-starved VCO scheme ensures energy efficiency and compact area, making it an ideal candidate for high-speed biomedical and mobile wireless sensors.

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