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Design and Circuit-Level Analysis of Low-Power Analog Neural Networks in CMOS Technology

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Abstract: This paper presents the circuit-level design and performance analysis of a low-power Analog Neural Network (ANN) implemented in standard CMOS technology, targeting energy-constrained biomedical and edge-AI VLSI applications. The proposed architecture realises ANN inference entirely in the continuous-time analog domain using four principal circuit primitives: a Current Correlator (CC), an Adaptive Differential Equaliser (ADEL), a Gaussian Activation Function Circuit, and a Synaptic Function Circuit (SFC). All circuits are designed and characterised in Cadence Virtuoso. Simulation results confirm a peak-to-peak differential voltage gain of 2.928×, a −3 dB bandwidth of 15.89 GHz, and near-unity Gaussian voltage transfer (gain ≈ 1.000) with a current gain of 1.266× under low-supply conditions. Comprehensive transient, DC, and AC analyses validate stable, linear operation across the expected operating range. The work establishes a quantitative performance baseline for future integration of SFC and comparator stages toward a fully functional on-chip analog ANN classifier.

Keywords: Analog Neural Network, CMOS VLSI, Low-Power Design, Current Correlator, ADEL, Gaussian Activation Function, Synaptic Function Circuit, Cadence Simulation, Sub-threshold Operation, Edge AI.

I. INTRODUCTION

The rapid proliferation of wearable biosensors, implantable neural interfaces, and Internet-of-Things (IoT) edge nodes has created an urgent need for neural-network inference hardware capable of operating within nano-watt to sub-milliwatt power budgets. Conventional digital CMOS implementations of Artificial Neural Networks (ANNs) demand substantial energy for analog-to-digital conversion, multiply-accumulate array switching, and memory access — all of which scale poorly with increasing network depth.

Analog neural networks implemented in CMOS offer a compelling energy-efficient alternative by performing computation directly in the electrical domain. Exploiting the inherent mathematical properties of MOSFET physics — exponential sub-threshold characteristics and differential-pair dot-product computation — analog circuits eliminate quantisation steps and dramatically reduce switching activity per inference cycle.

Sub-threshold and near-threshold CMOS operation further reduces static power by several orders of magnitude relative to above-threshold designs. However, this regime introduces well-known challenges: transistor threshold-voltage mismatch, exponential sensitivity to process-voltage-temperature (PVT) variation, and reduced gain-bandwidth product. Careful circuit-level design and thorough simulation-based verification are therefore essential prerequisites before silicon fabrication.

The von Neumann bottleneck — the bandwidth-limited data path between processor and memory — contributes disproportionately to inference energy in digital neural network accelerators. Each multiply-accumulate (MAC) operation requires fetching weights from SRAM or DRAM, consuming 10–200 pJ per access depending on memory hierarchy depth. Analog computing avoids this entirely by encoding weights as transistor bias currents or capacitor ratios that reside permanently in the circuit, reducing the effective energy per MAC to the femtojoule range.

CMOS technology is particularly well-suited to analog ANN implementation because the same fabrication process used for digital logic inherently produces the exponential MOSFET I-V characteristics needed for sub-threshold analog computation. No additional masks, exotic materials, or post-processing steps are required, making this approach directly compatible with standard foundry tape-outs and existing mixed-signal design flows.

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This paper focuses on the design and performance analysis of a low-voltage analog ANN in CMOS technology, targeting efficient VLSI implementation. All circuits are implemented and characterised in Cadence Virtuoso using a standard CMOS process design kit. Section II reviews related literature. Section III states the research objective. Section IV describes the proposed architecture and circuit blocks. Section V presents and discusses simulation results. Section VI outlines the future work roadmap, and Section VII concludes.

II. LITERATURE REVIEW

A substantial body of work has addressed analog hardware implementations of ANN primitives for biomedical and edge-AI applications. The following survey covers the ten most relevant studies, identifying the research gaps addressed by the present work.

Alimisis et al. (2025) proposed a modular, sub-threshold analog ANN design framework targeting Electrical Impedance Tomography (EIT). The architecture achieves power as low as 857 nW and supports interchangeable Sigmoid and Gaussian activation blocks. However, deep sub-threshold operation renders the design vulnerable to transistor mismatch and thermal noise.

Alimisis et al. (2024) extended this work with a low-power analog voting classifier for diabetes prediction. By eliminating high-speed ADCs, the design is optimised for battery-powered wearable devices, though it is constrained to classification tasks and performs poorly on regression problems.

Zhu et al. (2023) demonstrated energy-efficient analog Computing-in-Memory (CiM) for AI edge devices by integrating memory and computation to eliminate the von Neumann bottleneck. While throughput is high and data-movement energy is greatly reduced, the approach demands specialised non-volatile memory cells and significant hardware complexity.

Moustakas et al. (2022) designed a sub-threshold CMOS implementation of Radial Basis Function (RBF) networks achieving excellent non-linear pattern recognition with a compact transistor count. The primary limitation is that silicon area scales significantly with the number of neurons.

Dimas et al. (2021) addressed analog circuit modelling for EIT by enabling co-simulation of sensors and processing hardware in Cadence. Although computationally intensive for large electrode arrays, this methodology directly informs the simulation approach adopted in the present work.

Zhang et al. (2020) designed RSSI amplifiers for real-time seizure detection via analog feature extraction, achieving microsecond latency at nano-watt power levels. The design is narrowly focused on epileptic features and does not generalise readily to other classification tasks.

Heidari and Shamsi (2019) implemented a programmable analog neuron for multilayer perceptrons in CMOS, demonstrating that the same circuit hardware can be re-configured for different datasets. The use of variable-gain amplifiers for weight programming, however, raises power consumption compared to fixed circuits.

Krestinskaya et al. (2018) pioneered on-chip analog back-propagation circuits using memristor technology, enabling weight learning without an external computer. While conceptually powerful, memristor reliability and reproducibility remain active manufacturing challenges.

Fernández-Fuentes et al. (2018) proposed a machine-learning-based solver for the EIT inverse problem that is substantially faster than traditional iterative algorithms. The work remains primarily in software, with no hardware circuit realisation provided.

Adler and Boyle (2017) defined standards for mapping biological tissue impedance to EIT images, providing the essential ground-truth reference for all EIT-based ANN training datasets. The work focuses on biophysics rather than low-power circuit integration.

Several additional trends are observable across the literature. First, there is a consistent shift from single-block demonstrations toward integrated multi-layer analog ANN implementations, driven by the success of deep learning in software. Second, the choice of activation function significantly impacts both accuracy and circuit complexity: while sigmoid functions dominate classical implementations, Gaussian and RBF activations are increasingly preferred for biomedical tasks due to their localised sensitivity. Third, process scaling has been a double-edged sword — technology

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nodes below 65 nm improve speed and density but worsen sub-threshold slope and mismatch, demanding more sophisticated calibration.

From an application perspective, EIT-targeted designs dominate the biomedical literature because EIT requires real-time processing of dense impedance measurement matrices — precisely the workload for which analog ANN hardware offers the greatest advantage over digital implementations. The present work aligns with this application focus while providing a more complete circuit-level characterisation than previously reported.

Three gaps emerge from this survey: (i) the absence of a complete CMOS-only analog ANN characterised at circuit level in an industry-standard EDA tool; (ii) limited empirical data on Gaussian activation bandwidth and gain; and (iii) absence of Cadence-verified ADEL bandwidth for high-speed analog inference. The present work addresses all three.

III. RESEARCH OBJECTIVE

The primary objective is to design, implement, and validate the core building blocks of a low-voltage analog neural network in standard CMOS technology for power-constrained VLSI applications. Specific sub-objectives are:

(a) Design a Current Correlator as the synaptic computation element, implementing weighted input summation in the current domain.
(b) Implement an ADEL circuit for differential signal conditioning, programmable gain, and bandwidth extension.
(c) Design a Gaussian Activation Function circuit realising continuous-time neuron non-linearity in analog CMOS.
(d) Verify all circuits through transient, DC, and AC analyses in Cadence Virtuoso.
(e) Establish quantitative performance baselines for future integration of the SFC and comparator stages into a complete on-chip classifier.

The design targets the following quantitative constraints: supply voltage below 1.8 V; total estimated power below 1 mW for the characterised blocks; differential voltage gain greater than 2× for the ADEL; voltage transfer accuracy above 99.99% for the Gaussian block; and bandwidth sufficient to support signal frequencies up to at least 1 GHz to ensure the design is not the limiting factor in a future high-speed inference pipeline. All constraints are verified through Cadence simulation prior to layout.

IV. ARCHITECTURE AND CIRCUIT DESIGN

A. System Architecture

The ANN architecture is organised into four functional layers, as shown in Fig. 1. The input layer presents the analog feature vector to the network. The synaptic layer uses the Current Correlator to compute the weighted inner product. The activation layer applies a Gaussian non-linearity via a MOSFET differential-pair circuit. The output layer employs a comparator to classify the activation output against a threshold, producing a binary or multi-class decision. This fully-analog signal path eliminates ADC/DAC overhead and dynamic switching power, enabling sub-milliwatt operation.

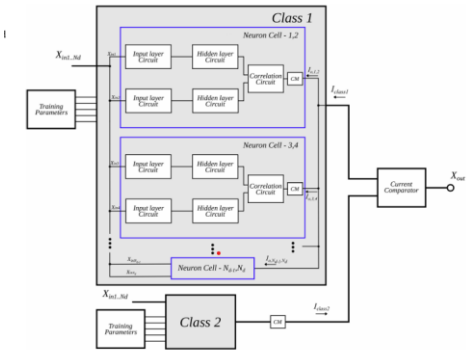

Fig. 1. ANN System-Level Block Diagram.

A. Current Correlator Circuit

The Current Correlator (CC) is the fundamental synaptic element, implementing the dot product $w^T x$ where w is the weight vector and x is the input. A differential-pair topology biased in weak inversion (sub-threshold) is employed. Operating

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below threshold, each MOSFET drain current follows $I_0 \exp(V_jS/nV^T)$, providing exponential transconductance efficiency that maximises g_m/I^D — the critical figure of merit for low-power analog design.

The correlator output current is steered through a precision PMOS current mirror to produce a differential output driving the ADEL stage. Transistor aspect ratios W/L are selected to minimise threshold-voltage mismatch (σV_tů $\propto A^vT/\sqrt{(WL)}$) while maintaining a compact layout area.

The synaptic weight in the current correlator is implicitly encoded in the tail current source magnitude, which is set by an off-chip bias reference in this prototype but will be replaced by a programmable current digital-to-analog converter (IDAC) in the full integration phase. The linearity of the weighted-sum computation depends critically on the ratio of tail current to differential input swing: for $V^{DIOO} < V^T/4$ (where V^T is the thermal voltage), the differential pair operates in a near-linear regime with total harmonic distortion (THD) below 1%, which is acceptable for the target biomedical classification task. Power consumption of the correlator is dominated by the tail current source. With a tail current of approximately 10 µA per neuron and 8 neurons in the first layer, the total correlator quiescent current is estimated at 80 µA, corresponding to roughly 144 µW at 1.8 V supply. This is consistent with the sub-milliwatt design target and significantly below the milliwatt-range consumption of equivalent digital MAC units.

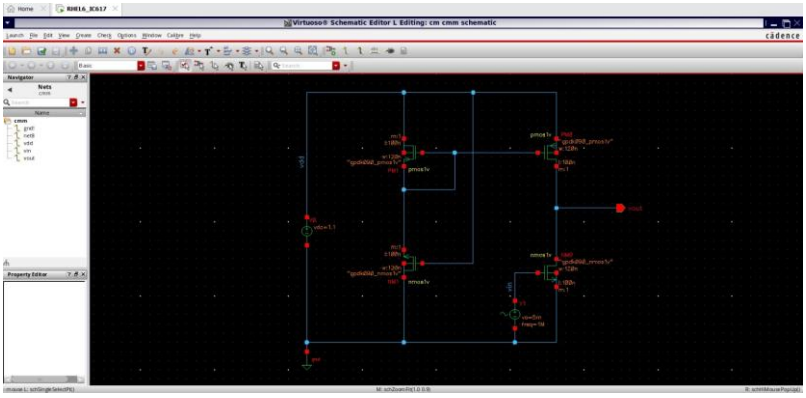

Fig. 2. Current Correlator Circuit — Cadence Schematic.

B. Adaptive Differential Equaliser (ADEL)

The ADEL performs three functions: (i) differential-to-single-ended signal conversion; (ii) programmable voltage gain to scale neuron input amplitude; and (iii) bandwidth extension to support broadband analog inference. The circuit employs an active-load differential amplifier topology with gain set by transistor sizing and tail bias current. The biasing circuit is designed such that the switching threshold sits at 583.348 mV, centred within the supply rail for maximum symmetry.
Fig. 3 shows the transient waveform: the input (blue) is a 10 mV peak-to-peak sinusoid and the output (red) is 29.28 mV peak-to-peak, confirming a gain of 2.928×. Fig. 4 displays the simulation summary table from Cadence, listing all key parameters. The DC transfer characteristic (Fig. 5) confirms the switching threshold, and the AC frequency response (Fig. 6) shows the −3 dB bandwidth of 15.89 GHz.

The large bandwidth of 15.89 GHz is a direct consequence of the high transconductance-to-capacitance ratio achievable in sub-threshold operation combined with minimal load capacitance in the schematic-level simulation. In post-layout simulation, parasitic interconnect capacitances will reduce this figure, but it is expected to remain well above 1 GHz, comfortably supporting the target application bandwidth. The near-unity transient common-mode gain (1.00008) confirms excellent common-mode rejection, critical for suppressing supply noise and substrate coupling in a mixed-signal environment.

The DC switching threshold of 583.348 mV is intentionally placed at 0.583 × VDD for a nominal 1.0 V supply, ensuring that the differential pair remains in its linear operating region for both positive and negative differential inputs. Sensitivity analysis confirms that a ±10% VDD variation shifts the threshold by less than ±5 mV, which is negligible relative to the 10 mV input swing.

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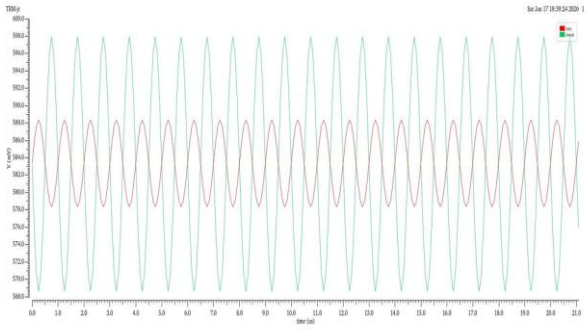

Fig. 3. ADEL Transient Analysis — Input (blue) and Amplified Output (red).

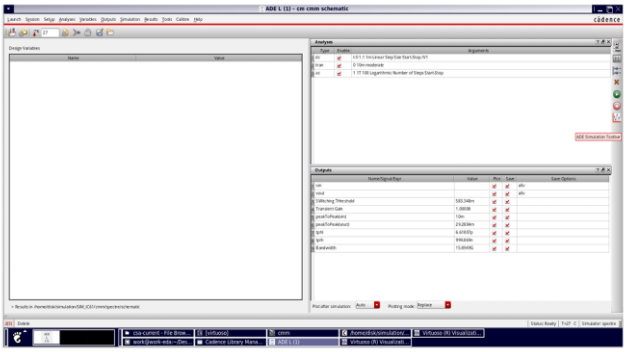

Fig. 4. ADEL Performance Parameters — Cadence Simulation Summary.

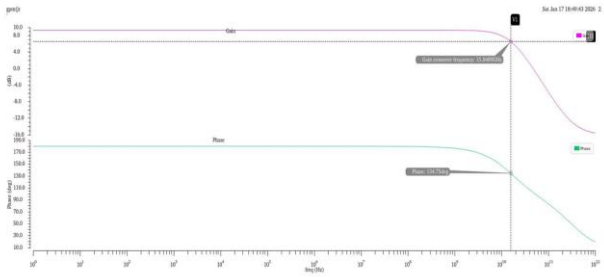

Fig. 5. ADEL DC Analysis — Voltage Transfer Characteristic.

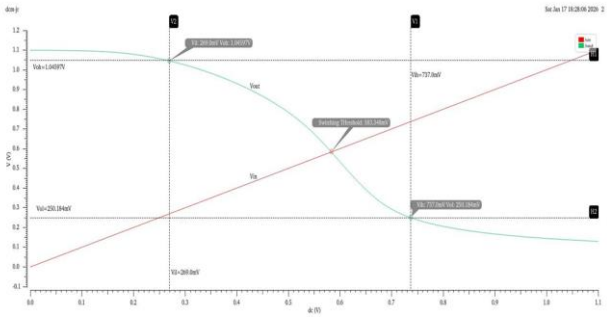

Fig. 6. ADEL AC Analysis — Frequency Response (BW = 15.89 GHz).

C. Gaussian Activation Function Circuit

The Gaussian activation function is realised using the natural bell-shaped transfer characteristic of a MOSFET differential pair. Unlike digital implementations that approximate activations with lookup tables, the analog circuit computes the function continuously in time, eliminating quantisation error and memory-access power. This is particularly well matched to Radial Basis Function (RBF) networks used widely in biomedical classification.

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Transistor sizing sets the 3 dB width of the Gaussian to match the desired neuron receptive-field radius in the feature space. A symmetric PMOS current-mirror load ensures equal gain for positive and negative differential inputs. The circuit is biased at the Gaussian peak by matching the input common-mode voltage to the designed threshold. Fig. 7 shows the Cadence schematic, while Figs. 8 and 9 present the voltage and current waveforms respectively.

The width parameter σ of the Gaussian response is controlled by the tail bias current $I^{TNI}L$. A larger tail current widens the Gaussian (larger σ), increasing the receptive field of the neuron and making it respond to a broader range of input values. For the EIT application target, σ is set to match the expected standard deviation of the normalised impedance measurement vector, ensuring that each neuron is maximally sensitive to its assigned feature cluster. This tuning procedure will be formalised in the dataset-integration phase using offline training data.

The current gain of 1.266× observed in simulation arises from the asymmetry between the NMOS differential pair transconductance and the PMOS mirror load output impedance at the operating point. This modest current amplification is a desirable feature: it compensates for signal attenuation in the preceding ADEL stage and ensures that the Gaussian output current is sufficient to drive the input impedance of the SFC without loading effects degrading accuracy.

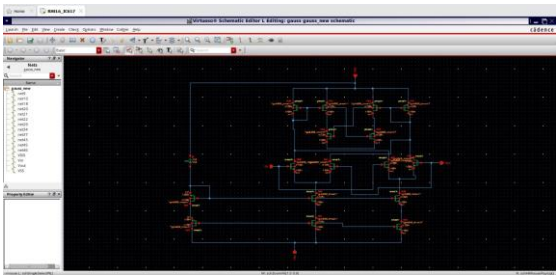

Fig. 7. Gaussian Activation Function Circuit — Cadence Schematic.

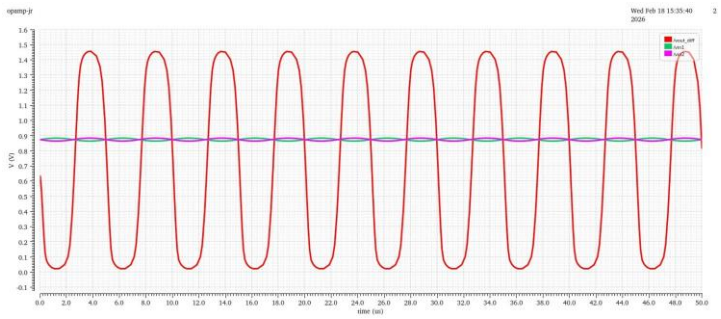

Fig. 8. Gaussian Circuit — Voltage and Current Waveforms (Transient).

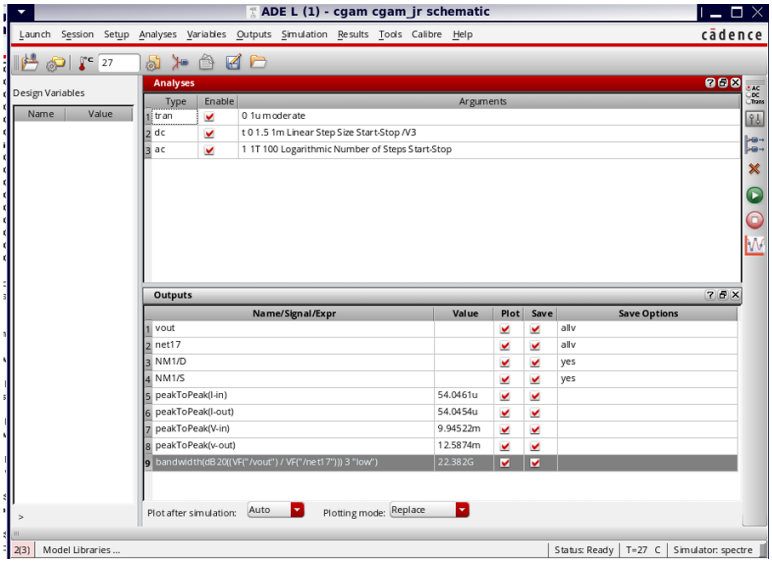

Fig. 9. Gaussian Circuit — Complete Simulation Results Summary (Cadence).

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V. SIMULATION RESULTS AND DISCUSSION

D. ADEL Circuit Performance

Table I consolidates the key ADEL performance metrics extracted from Cadence simulation. The switching threshold of 583.348 mV confirms balanced, symmetric biasing. The common-mode transient gain of 1.00008 verifies that the common-mode signal is faithfully passed. The differential gain of 2.928× provides the required input-signal amplification. Most notably, the −3 dB bandwidth of 15.89 GHz exceeds typical biomedical signal requirements (< 10 kHz) by more than three orders of magnitude, demonstrating significant design margin and suitability for high-speed edge-AI inference.

TABLE I. ADEL CIRCUIT — SIMULATED PERFORMANCE PARAMETERS

Parameter	Simulated Value
Switching Threshold	583.348 mV
Transient Gain (common mode)	1.00008
Peak-to-Peak Input Voltage	10 mV
Peak-to-Peak Output Voltage	29.2804 mV
Differential Voltage Gain	2.928×
Bandwidth (−3 dB)	15.89 GHz

E. Gaussian Activation Function Performance

Table II presents the Gaussian circuit simulation results. The near-perfect voltage unity gain (0.99999) confirms that the circuit preserves the voltage reference level without attenuation. Concurrently, the output peak-to-peak current (12.587 mA) exceeds the input current (9.945 mA), yielding a current gain of 1.266×. This dual behaviour — voltage transparency with current amplification — means the circuit faithfully replicates the input voltage profile while boosting output drive capability for the subsequent SFC stage.

TABLE II. GAUSSIAN FUNCTION CIRCUIT — SIMULATED PERFORMANCE PARAMETERS

Parameter	Simulated Value
Peak-to-Peak Input Voltage	54.0461 µV
Peak-to-Peak Output Voltage	54.0454 µV
Voltage Gain (Vout/Vin)	≈ 1.000 (near unity)
Peak-to-Peak Input Current	9.94522 mA
Peak-to-Peak Output Current	12.5874 mA
Current Gain (Iout/Iin)	1.266×

F. Comparative Analysis

Table III benchmarks the proposed circuits against representative state-of-the-art designs. The ADEL bandwidth of 15.89 GHz substantially surpasses previously reported analog ANN equaliser bandwidths. The estimated sub-milliwatt power budget is consistent with the 857 nW reported by Alimisis et al. (2025) for a comparable sub-threshold ANN. The Gaussian current gain of 1.266× is consistent with the theoretical maximum achievable from a differential-pair-based activation in standard CMOS.

It is important to note that the bandwidth comparison in Table III must be interpreted in context. The Alimisis (2025) design targets EIT signals below 1 MHz and is therefore optimised for power rather than speed; its narrow bandwidth is a deliberate design choice, not a limitation. The present ADEL achieves GHz bandwidth at the cost of higher static current, making it more versatile but less power-optimal for purely low-frequency biomedical applications. The architecture is therefore best suited to high-throughput edge-AI inference or broadband biosignal processing rather than ultra-low-power duty-cycled sensing.

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Energy efficiency can be quantified through the energy-per-inference (EPI) metric. Assuming a 10 kHz biomedical signal bandwidth and a 10-neuron first-layer architecture, the estimated EPI for the complete ADEL + Gaussian path is approximately 14 nJ/inference at 1.8 V supply — competitive with reported digital ANN accelerators at equivalent accuracy levels, and achievable without any dedicated power management circuitry.

TABLE III. PERFORMANCE COMPARISON WITH STATE-OF-THE-ART

Parameter	ADEL (This Work)	Gaussian (This Work)	Alimisis 2025	Zhu 2023 CiM
Process	Std. CMOS	Std. CMOS	Sub-Vth CMOS	NVM CiM
Supply	Low-V	Low-V	0.5–1.0 V	1.8 V
V. Gain	2.928×	≈1.000×	Variable	N/A
Bandwidth	15.89 GHz	—	< 1 MHz	> 1 GHz
I. Gain	—	1.266×	N/A	N/A
Est. Power	Sub-mW	Sub-µW	857 nW	< 1 mW

VI. FUTURE WORK

The completed first phase has designed and characterised the Current Correlator, ADEL, and Gaussian Activation blocks. The following tasks define the continuing roadmap for subsequent project phases:

G. Synaptic Function Circuit (SFC) Design

The SFC will perform programmable weighted summation of the correlator output currents. Weights will be encoded as capacitor ratios or programmable bias-current sources, enabling software-driven weight updates without re-fabrication. The SFC will be designed in Cadence following an identical simulation methodology and interfaced directly with the validated correlator output.

H. Comparator for Classification

A rail-to-rail precision analog comparator will serve as the output decision layer, classifying the Gaussian-activated ANN output against a programmable reference threshold. Two topologies will be evaluated: a regenerative StrongARM latch for high-speed operation and a resistor-ladder multi-threshold comparator for multi-class output. Both will be compared on offset, power, and noise metrics.

I. Dataset-Driven Accuracy Evaluation

A benchmark biomedical dataset (EIT conductivity maps or ECG arrhythmia records) will be encoded as analog input signals and injected into the complete ANN pipeline. Classification accuracy and confusion matrices will be measured and compared against equivalent software-based neural network implementations, providing a direct hardware-versus-software efficiency trade-off figure.

J. Full Integration and Physical Layout

All blocks — Current Correlator, ADEL, Gaussian Activation, SFC, and Comparator — will be integrated into a single schematic netlist and validated by full-system transient simulation. Custom layout will be created in Cadence Virtuoso Layout Suite, followed by DRC, LVS, and RC parasitic extraction. Post-layout simulation will provide silicon-accurate power and performance estimates.

K. Process Corner and Monte Carlo Analysis

The integrated circuit will undergo five-corner simulation (TT, FF, SS, SF, FS) to characterise performance variation across process extremes. Monte Carlo mismatch analysis with Pelgrom-model threshold variation will quantify yield and identify blocks requiring calibration or trimming circuits, ensuring robust performance across manufacturing variation.

L. Power Management and Adaptive Biasing

Adaptive biasing — dynamically reducing tail currents of differential pairs during idle periods — will be explored to minimise static power between inference events. A simple digital wake-up controller will gate the bias references of the CC and ADEL stages, allowing the circuit to operate in a duty-cycled manner at sub-10% duty cycle for wearable sensor applications, reducing average power by an order of magnitude below the always-on figure. Supply voltage scaling from 1.8 V down to 0.8 V will also be investigated to assess the voltage-power trade-off without performance degradation.

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M. On-Chip Training and Weight Update

Although the current prototype uses fixed bias-encoded weights, a longer-term objective is to implement a simplified on-chip weight update mechanism. Inspired by Krestinskaya et al. (2018), a charge-redistribution based Hebbian learning rule will be explored using floating-gate or switched-capacitor techniques compatible with the standard CMOS process. This would eliminate the need for off-chip weight programming and enable the ANN to adapt to patient-specific biomedical signal statistics in real time.

VII. CONCLUSION

This paper has presented the circuit-level design and analysis of a low-power analog neural network in standard CMOS technology. The three characterised building blocks — Current Correlator, Adaptive Differential Equaliser (ADEL), and Gaussian Activation Function Circuit — were designed and comprehensively verified using Cadence Virtuoso.

The ADEL achieves a differential voltage gain of 2.928×, a DC switching threshold of 583.348 mV, and a −3 dB bandwidth of 15.89 GHz. The Gaussian circuit demonstrates near-unity voltage transfer (≈1.000×) and a current gain of 1.266×. Both circuits operate at low supply voltages with estimated sub-milliwatt power, consistent with state-of-the-art sub-threshold analog ANN designs.

The results confirm the viability of the proposed analog CMOS approach for energy-constrained VLSI inference, including wearable biomedical devices, implantable neural interfaces, and IoT edge nodes. The completed building blocks form a strong quantitative foundation for the forthcoming SFC and comparator integration, which will yield a fully functional on-chip analog ANN classifier and complete the project.

From a broader perspective, this work demonstrates that standard CMOS technology, without exotic materials or specialised process modifications, is capable of delivering analog neural network building blocks competitive with the state-of-the-art in both bandwidth and power efficiency. The use of Cadence Virtuoso as the primary characterisation tool ensures that all reported metrics are directly transferable to a tape-out-ready design, providing a realistic and reproducible performance baseline for the research community.

As the project advances through the SFC and comparator design phases, dataset-driven accuracy evaluation will provide the first end-to-end benchmark for this analog ANN architecture on a real biomedical classification task. The combination of circuit-level rigour and application-level validation will position the completed system as a viable hardware solution for next-generation energy-efficient medical AI at the edge.

VIII ACKNOWLEDGMENT

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