IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

Impact Factor 8.311 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 13, Issue 5, May 2026

DOI: 10.17148/IARJSET.2026.13518

Design and Implementation of a 10-bit FSM based Digital SAR Logic in 90 nm CMOS Technology

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Abstract: In mixed-signal systems, analog to digital converters (ADCs) are crucial for transforming analog signals into digital data. The Successive Approximation Register (SAR) ADC is one of the most popular ADC architectures because of its low power consumption, moderate resolution, and straightforward hardware design, which make it appropriate for Internet of Things applications, portable electronics, and biomedical devices. The control unit that completes the successive approximation process to produce the final digital output is the digital SAR logic.

In this work, a 10-bit Finite State Machine (FSM) based digital SAR logic using 90 nm CMOS technology is designed and implemented. The binary search conversion from the Most Significant Bit (MSB) to the Least Significant Bit (LSB) is carried out by the suggested architecture.

The Cadence digital design flow, which includes synthesis, timing analysis, power estimation, and physical design processes like floor planning, placement, routing, and GDSII generation, is used to create the design. The results show low power consumption and effective area utilization. For integration in low-power SAR ADCs used in biomedical, wireless sensor, and embedded data acquisition systems, the suggested FSM-based SAR logic provides a small and energy-efficient solution.

Keywords: Successive Approximation Register (SAR), Finite State Machine (FSM), Digital SAR Logic, Verilog HDL, 90 nm CMOS Technology, Low-Power VLSI Design, Analog-to-Digital Converter (ADC).

I. INTRODUCTION

The need for effective data conversion methods that can interface analog signals from the real world with digital processing systems has greatly increased due to the quick development of digital electronics and embedded systems. Modern electronic systems process data digitally, but the majority of natural signals, including temperature, sound, pressure, and biomedical signals, exist in analog form. Analog-to-Digital Converters (ADCs) are therefore essential for bridging the gap between digital processing units and analog environments. Biomedical instrumentation, wireless communication systems, sensor networks, industrial monitoring systems, and Internet-of-things (IoT) devices are just a few of the numerous applications for ADCs.

Over time, a number of ADC architectures have been created, such as flash ADCs, pipeline ADCs, sigma-delta ADCs, and Successive Approximation Register (SAR) ADCs. Because of its low power consumption, straightforward structure, and effective conversion mechanism, the Successive Approximation Register (SAR) ADC has emerged as one of the most widely used architectures for medium-speed and moderate-resolution applications. Because SAR ADCs use a binary search algorithm for conversion instead of large parallel comparators as flash ADCs do, they usually achieve high energy efficiency.

A sample-and-hold circuit, comparator, digital-to-analog converter (DAC), and SAR control logic are some of the essential parts of the SAR ADC architecture. The digital SAR logic serves as the main control unit among these blocks, coordinating the conversion process as a whole. By comparing the input analog voltage with the reference voltage produced by the DAC, the SAR logic sequentially determines each bit of the digital output. The SAR logic uses a binary search algorithm to approximate the input signal with high accuracy, starting from the Most Significant Bit (MSB) and moving toward the Least Significant Bit (LSB).

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Conventional SAR control logic implementations use complex combinational circuits together with asynchronous control schemes for their control operations. The two methods achieve correct operation but they result in greater hardware complexity together with increased silicon requirements and higher energy usage. The restrictions become especially important for contemporary portable electronic devices which require both minimal power usage and small form factor as essential design requirements. The ongoing miniaturization of technology raises the necessity for efficient digital control logic design to enhance overall performance of SAR ADC systems.

To solve these problems, designers should use Finite State Machine (FSM) digital design techniques to build their SAR control logic. The Finite State Machine enables digital circuits to control their sequential processes through its defined framework. The FSM-based SAR logic system uses multiple operational states which include initialization, sampling, conversion, and completion to enhance control circuitry efficiency while achieving better system dependability and reduced power consumption during operation. Digital systems which use Hardware Description Languages like Verilog HDL enable efficient SAR control logic design through their ability to model, verify, and synthesize modern CMOS technology systems.

This work presents a digital SAR design which uses 10-bit FSM-based technology that operates on 90-nanometer CMOS devices. The proposed design utilizes a structured FSM architecture to control the successive approximation process efficiently. The digital output system determines each bit through its interactions with comparator and DAC control signals. The design is implemented using Verilog HDL and verified through RTL simulation to ensure correct functionality of the conversion algorithm.

The digital SAR logic is synthesized using Cadence digital design tools, and the implementation follows a standard ASIC design flow including logic synthesis, timing analysis, and physical design stages such as floor planning, power planning, placement, routing, and layout generation. The proposed architecture achieves its design goals through three main features which include low power consumption, effective area utilization, and dependable operation together with accurate SAR conversion control.

The remainder of this paper follows this organizational structure. Chapter 2 presents the literature review of existing research works related to SAR ADC architectures and digital SAR control logic implementations. Chapter 3 discusses the existing methodology and conventional SAR logic operation used in ADC systems. Chapter 4 presents the proposed methodology, which includes the architectural design of 10-bit FSM-based digital SAR logic and its functioning principles. Chapter 5 presents the simulation results and performance analysis of the proposed SAR logic design. Chapter 6 concludes the paper and suggests future research directions, which are followed by the reference list.

II. LITERATURE REVIEW

The Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) has become one of the most widely used ADC architectures for low-power and medium-speed applications because it has a simple design which uses less energy and achieves moderate conversion speeds. Researchers have developed various SAR ADC designs together with digital control methods which enhance power usage and speed up conversion times while boosting system dependability.

Dina M. Ellaithy (2024) developed a power-efficient 8-bit SAR ADC which uses 130 nm CMOS technology to create a biomedical and wearable device application. The design includes a sample-and-hold circuit together with a comparator and a capacitive DAC and the SAR control logic. The design team aimed for low energy usage because they wanted to reach dependable conversion results. The SAR logic applies the binary search method to identify each bit from the most significant bit (MSB) down to the least significant bit (LSB). The proposed design demonstrates efficient power utilization which makes it appropriate for portable medical monitoring systems. The design uses basic SAR control logic which limits its ability to achieve higher resolution.

De La Fuente-Cortes et al. (2024) created a non-linear successive approximation finite state machine (FSM) which improves the SAR conversion process by enhancing its ADC robustness. The proposed FSM modifies the approximation sequence to enhance system stability and performance under different operating conditions. The design utilizes a structured state-machine-based control mechanism which enhances system reliability while decreasing the likelihood of conversion mistakes. The FSM-based system improves SAR control system stability but it makes the digital control system more difficult to operate.

Chen et al. (2025) presented a high-speed pipeline-SAR ADC architecture capable of achieving a sampling rate of 2.1 GS/s. This architecture incorporates the benefits of both pipeline and SAR conversion techniques. The conversion speed

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DOI: 10.17148/IARJSET.2026.13518

is improved by using optimized SAR logic and speed-enhanced bootstrap switches. This results in a faster conversion speed, which is useful for high-speed communication. However, the complexity of the combined pipeline-SAR ADC is high, resulting in increased power consumption.

Shehzad et al. (2021) presented a low-power asynchronous SAR ADC with a resolution of 12 bits, operating at a frequency of 20 MS/s. This architecture is useful for sensor-based applications. The asynchronous control logic is incorporated in the ADC architecture, which avoids the use of a global clock signal. This results in faster conversion speed and reduced power consumption. Although the conversion speed is improved, asynchronous control logic is complex and results in increased power consumption.

Banik et al. (2021) proposed a low power 6-bit SAR ADC using 90nm CMOS technology for biomedical applications in their paper "A Low Power 6-Bit Successive Approximation Type Analog-to-Digital Converter Using 90nm CMOS Technology" in 2021. The design is focused on reducing power consumption while ensuring proper conversion accuracy. The SAR controller is designed using conventional digital control for successive approximation. The design is reliable in terms of power consumption but is not appropriate for high-precision data acquisition systems due to low resolution and conventional SAR control logic.

From a review of these references, it is noted that most SAR ADC design methodologies are mainly concentrated on optimizing various analog circuits such as DAC array and comparator circuits, and digital SAR control logic is often implemented using conventional methods. Moreover, some design methodologies have concentrated more on high-speed design and/or asynchronous design, which may lead to increased design complexity. Therefore, there is a need for developing a more efficient digital SAR control logic that ensures a more organized control mechanism for the SAR conversion process with low design complexity and power consumption. In order to fill this gap in the existing literature, this work proposes a 10-bit FSM-based digital SAR logic implemented in 90 nm CMOS technology.

III. EXISTING METHODOLOGY

The conventional Successive Approximation Register (SAR) Analog-to-Digital Converters are based on the control logic implemented using the analog-based SAR. In the conventional SAR ADCs, the control of the conversion process is carried out by using the basic registers and the analog-based control logic. In the reference design considered for this work, an analog-based SAR logic control architecture is used. The reference design considered for this work is based on the analog-based SAR logic control architecture implemented using the CMOS technology.

The SAR ADC uses a binary search algorithm to convert an input analog signal into a digital output signal. The Analog SAR logic dictates the step-by-step process of comparing the sampled input voltage and the reference voltage produced by the Digital-to-Analog Converter (DAC). This control process generates each bit of the output signal sequentially from the Most Significant Bit (MSB) to the Least Significant Bit (LSB).

3.1 Analog SAR Logic

In a conventional SAR ADC architecture, the logic control of the SAR is carried out through analog control logic and simple shift registers. The analog control logic controls the sequence of operations during the conversion process. This logic controls the selection of different capacitors in the CDAC and also controls the decision of the comparator. The conversion process begins with a trial on the MSB bit. In this case, the logic control of the SAR sets the MSB bit to logic '1,' and a reference voltage corresponding to this bit is generated at the DAC output. This reference voltage is compared to the input voltage, and a decision is made whether to maintain it at logic '1' or reset it to logic '0.'

3.2 Operation of Analog SAR Conversion

The operation of the analog SAR conversion may be explained as follows:

1. Sampling Phase
   The input signal is stored in the sampling capacitor. This is the first step in the conversion process.
2. MSB Approximation
   The MSB is set to '1'. The DAC output voltage is half the reference voltage.
3. Comparison Phase
   The input voltage and the DAC output voltage are compared by the comparator.
4. Bit Decision
   The bit is set to '1' if the input voltage is higher than the DAC output voltage; otherwise, the bit is reset to '0'.
5. Successive Bit Approximation
   The same steps are repeated for all the bits starting with the MSB and ending with the LSB.

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6. Digital Output Generation
   The output code is generated after all the bits are approximated.

3.3 Limitations of Analog SAR Logic

Although the analog SAR logic guarantees reliable operation, there are a few limitations associated with the conventional design of the SAR ADC.

- Analog control circuits add to the complexity of the design process.
- Analog circuits are more susceptible to noise and process variations.
- The power consumption may increase with the analog switching circuits.
- The proposed architecture is not easily scalable for higher resolution ADC design.
- The analog nature of the proposed logic makes it difficult to integrate with the digital design process.

To overcome the limitations associated with the analog SAR logic, the recent SAR ADC design uses a fully digital SAR control logic.

IV. PROPOSED METHODOLOGY

To overcome the limitations of the traditional analog SAR control logic, a new approach based on the use of a Finite State Machine (FSM) for the design of the SAR logic is proposed in this paper. The proposed design of the SAR logic is based on the use of a structured FSM architecture.

The logic for the proposed SAR is intended for a 10-bit resolution, and the design is coded using Verilog Hardware Description Language (HDL) with a 90 nm CMOS process. The FSM-based architecture is intended to provide a sequence of control while keeping the design complexity low.

4.1 FSM Architecture of Digital SAR Logic

The digital SAR controller is implemented using a four-state Finite State Machine. The states used in the design are:

1. IDLE State
2. SAMPLE State
3. CONVERT State
4. DONE State

These states coordinate the entire analog-to-digital conversion process.

The FSM changes states according to the clock signal, reset signal, start signal, and output of the comparator. The SAR logic generates essential signals such as sample, hold, DAC, and End of Conversion (EOC).

4.2 State Diagram Explanation

The state diagram shown in the Fig. 1 represents the sequential operation of the SAR logic controller.

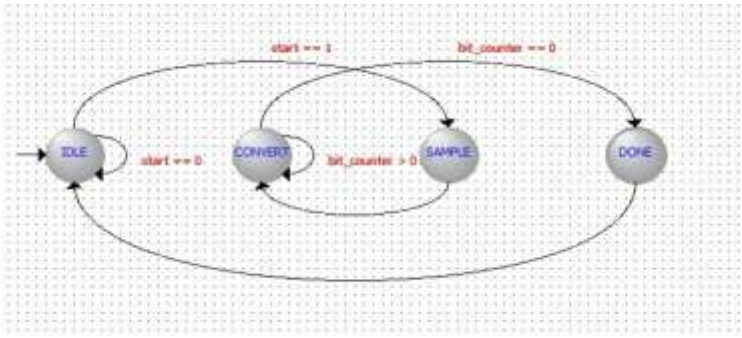

Fig. 1 State Diagram

IDLE State

The system is initially in the IDLE state. In the IDLE state, the SAR logic waits for the start signal to start the conversion process. The sampling signal is not active, and the hold signal is active to ensure the stability of the system.
When the start signal is high, the system changes from the IDLE state to the SAMPLE state.

SAMPLE State

In the SAMPLE state, the input given in the form of an analog signal is picked up by the sample and hold circuit. The sampling signal is activated, and the input signal is stored in the sampling capacitor.

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After the sampling is done, the FSM automatically goes to the CONVERT state and starts the succession of the approximation process.

CONVERT State

The CONVERT state carries out the main conversion task for the SAR. In this state, the logic of the SAR is used for the conversion of the bits of the output.

The SAR register sets the MSB (Most Significant Bit) to logic '1'. Then the DAC produces the reference voltage. The comparator compares the input voltage with the output voltage.

Based on the output of the comparator:

If the input voltage is higher than the DAC voltage, then the bit is set to logic '1'. Otherwise, the bit is reset to logic '0'. This process continues for all bits, starting from the MSB bit to the LSB bit. A bit counter is used to keep track of the number of bits left to process. Once all bits have been processed, the FSM changes to the DONE state.

DONE State

This state shows that the process of conversion using the SAR method is complete. At this time, the output code is available, which is stored in the SAR register. An EOC signal is generated to show that the conversion process is done. Then, the FSM changes back to the IDLE state, waiting to process the next start signal.

4.3 State Table Explanation

The state table defines the transitions between the different FSM states based on the input conditions.

Source State	Condition	Destination State
IDLE	Start = 0	Idle
	Start = 1	Sample
Sample	Next Cycle	Convert
Convert	Bit_counter== 0	Done
	Bit_counter > 0	Convert
Done	Next Cycle	Idle

Table 1 State Table

The state table given in Table 1 clearly illustrates the control flow of the SAR logic and ensures that each operation is performed in a particular sequence.

4.4 SAR Conversion Algorithm in the Proposed Design

The FSM-based SAR logic follows the binary search algorithm for analog-to-digital conversion.

The conversion steps are summarized as follows:

1. The input analog signal is sampled during the SAMPLE state.
2. The SAR register sets the MSB to logic '1'.
3. The DAC generates a corresponding reference voltage.
4. The comparator compares the sampled input voltage with the DAC output.
5. Based on the comparator output, the bit is retained or cleared.
6. The SAR logic moves to the next lower bit.
7. This process continues until all bits are determined.
8. The final digital output is produced during the DONE state.

4.5 Advantages of FSM-Based SAR Logic

The proposed digital logic implementation of the SAR logic using an FSM has several advantages compared to a conventional analog control circuit for a SAR logic.

- Low power consumption due to a digital implementation
- Low hardware complexity
- Improved reliability and stability
- Easier integration into a digital ASIC design flow

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DOI: 10.17148/IARJSET.2026.13518

- Easier scalability to a high-resolution ADC system

The use of an FSM architecture allows the SAR control logic to function effectively while ensuring accurate and reliable conversion.

V. RESULTS AND DISCUSSION

This chapter discusses the simulation results of the proposed 10-bit FSM-based digital SAR logic implementation. The implementation results of the proposed 10-bit FSM-based digital SAR logic are presented in this chapter. The implementation results are carried out in Verilog HDL, and the Cadence digital flow is used to verify it.

5.1 RTL Simulation Results

The functionality of the proposed SAR logic is verified by RTL simulation. The simulation results confirm the correct functionality of the Finite State Machine (FSM) and the successive approximation algorithm used in the SAR ADC.

During the simulation process, the following signals were analyzed:

- Clock signal
- Reset signal
- Start signal
- Comparator output
- SAR register output
- End-of-Conversion (EOC) signal

The Finite State Machine is initially in the idle state until the start signal is enabled. When the start signal is enabled, the Finite State Machine moves to the sample state. In the sample state, the analog input is sampled. The system then moves to the convert state, where the SAR logic determines each bit one by one starting from the Most Significant Bit (MSB) to the Least Significant Bit (LSB).

In each clock cycle, the SAR register updates the value of the bits based on the output of the comparator. The conversion is completed once all the bits are resolved. The Finite State Machine then moves to the done state, and the End of Conversion signal is issued to indicate that the digital output is ready.

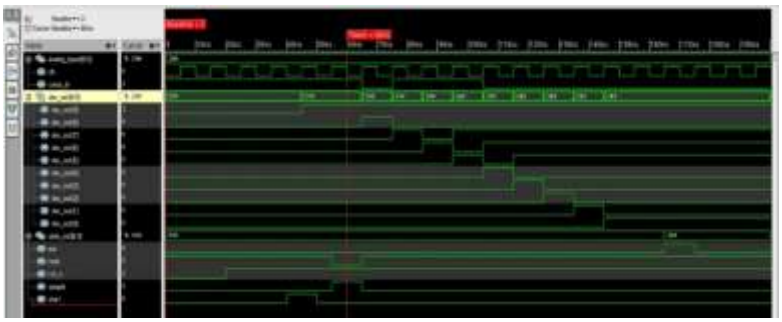

Fig 2 RTL Simulation

The waveform as shown in the Figure 5.1 above confirms the proper operation of the SAR conversion process and the proper transitions of the FSM states.

5.2 Synthesis Results

The RTL code was synthesized using a 90nm CMOS standard cell library. The synthesis of the code transforms the behavioral Verilog code into a netlist of logic gates and flip-flops.

The synthesis tool performs several optimizations to achieve:

- Reduced area
- Low power consumption
- Improved timing performance

The table 2 shows the synthesis report provides key design metrics such as total cell count, area utilization, and power consumption.

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Parameter	Value
Technology	90 nm
Resolution	10-bit
Area	1257.968 μm^2
Power	0.02545 μW
Standard Cells	137 cells

Table 2 Synthesis Report

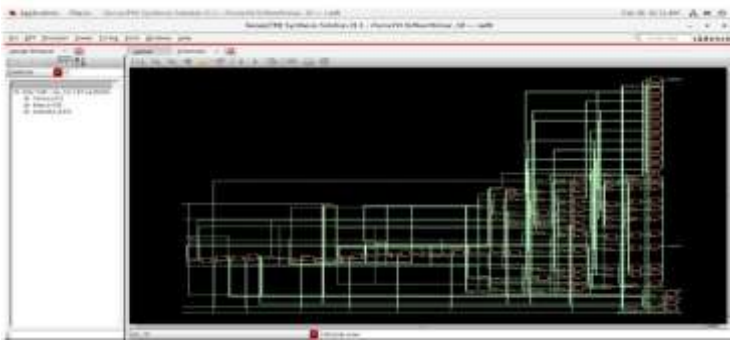

Fig 3 RTL of the SAR Logic

The synthesis results shown in Fig 3 indicate that the proposed architecture efficiently utilizes hardware resources.

5.3 Comparison with Existing Works

In order to validate the effectiveness of the proposed FSM-based digital SAR logic, the proposed design is compared with several existing SAR ADC architectures. The comparison has been carried out based on the resolution, technology node, chip area, and power consumption.

Title of the Paper	Resolution	Technology	Area	Power
Non-Linear Successive Approximation FSM for ADCs	10-bit	180 nm	0.12 mm²	1.2 mW
A Low-Power 12-bit 20-MS/s Asynchronously Controlled SAR ADC	12-bit	65 nm	0.14 mm²	472.2 µW
A 12-bit 20-MS/s Asynchronous SAR ADC With Background Calibration	12-bit	90 nm	0.09 mm²	620 µW
Design of SAR ADC Control Logic Using Verilog HDL	10-bit	90 nm	0.07 mm²	550 µW
Proposed Work: 10-bit FSM-Based Digital SAR Logic	10-bit	90 nm	1257.968 μm^2	0.02545 μW

Table 3 Comparison of the Existing and Proposed Work

5.4 Discussion

The RTL simulation and synthesis results show that the proposed FSM-based 10-bit digital SAR logic works successfully. It passes through all required states such as IDLE, SAMPLE, CONVERT, and DONE states which indicate correct control of the SAR. The register value is also updated successfully depending on the output of the comparator indicating successful execution of the binary search from the most significant bit to the least significant bit.

The synthesis results show that the designed digital SAR logic consumes low power and also makes reasonable usage of the area by using a standard cell library of 90 nm CMOS technology. It is evident that FSM-based control of the design simplifies the design more than analog SAR logic since it ensures the reliability of the design.

VI. CONCLUSION AND FUTURE WORK

6.1 Conclusion

This paper demonstrated the design and RTL realization of 10-bit FSM-based digital SAR logic using Verilog HDL in 90nm CMOS technology. The design proposed in this paper makes use of an FSM-based technique rather than a regular analog control mechanism for the implementation of the sequential steps in the SAR conversion process.

IARJSET ISSN (O) 2393-8021, ISSN (P) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

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The working of the design was validated by conducting the RTL simulation, which proves proper state transitions and bit-wise conversion of MSB to LSB. Synthesis reveals that the design is capable of delivering low power usage and good hardware utilization.

In summary, the proposed FSM-based digital SAR logic presents a simple and reliable method of designing a digital SAR ADC controller that can be extended to be used in future physical design implementation in fields like biomedical and sensor-based applications.

6.2 Future Work

The future scope of this research includes expanding the FSM-based digital SAR logic design from RTL level to physical ASIC implementation, which will involve steps such as floor planning, power planning, placement, CTS, and routing using commercial EDA tools. Optimization can further be done to enhance timing, minimize power, and reduce area by employing techniques such as clock gating and congestion-aware placement. Post layout verification methods like STA, DRC, and LVS can be applied to validate the design for manufacturing. Also, the proposed design can be fabricated using advanced CMOS technologies and can be combined with analog circuits such as DAC and comparator to form an entire SAR ADC system.

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