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Design and Comparative Analysis of 6T CMOS SRAM Cell Across Various Technology Nodes

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Abstract: This paper presents a comprehensive design and comparative performance analysis of a conventional 6-transistor (6T) CMOS static random-access memory (SRAM) cell implemented across four advanced CMOS technology nodes: 120 nm, 90 nm, 70 nm, and 50 nm. The SRAM cell architecture comprises two cross-coupled inverters and two access transistors, designed under identical specifications to systematically isolate the effects of technology scaling. Layout design and transient circuit simulations were conducted using Microwind VLSI design tool with BSIM4 transistor models to characterise cell behaviour during read and write operations. BSIM4 models enable accurate representation of device-level effects including leakage current and short-channel phenomena, which become increasingly prominent in scaled technologies. The analysis focuses on two critical performance metrics: dynamic power consumption and physical layout area. Results demonstrate that both power dissipation and silicon area decrease monotonically with technology node reduction. Specifically, the 50 nm implementation achieves the lowest power consumption and most compact layout, while the 120 nm node exhibits comparatively higher values. These findings elucidate the impact of technology scaling on fundamental SRAM characteristics and provide quantitative insights to inform efficient memory design and optimization in modern VLSI and system-on-chip implementations.

Keywords: 6T SRAM, CMOS Technology, Microwind, Power Consumption, Cell Area, Technology Scaling, VLSI Design, Nano Technology Nodes, Memory Management.

I. INTRODUCTION

Today's world, which is very much demand oriented for high performance and energy efficient electronic systems memory design has become a key element in modern VLSI and SoC development. We see processors getting more complex and faster the need for fast and reliable on chip memory has greatly grown. In this context, Static Random Access Memory (SRAM) is very important, especially in cache memories and embedded applications, which require fast data access and low latency to improve the overall performance of the system. Also its compatibility with standard CMOS processing which is a plus point for large scale integration.

During the past few decades, CMOS technology has been continuously scaled, resulting in higher transistor density and improved computational power. But with this scaling we have also introduced some problems which in turn affect the memory circuits. As device dimensions have been reduced we see increase in leakage current, variation in threshold voltage and reduced gate control over the channel which in turn play a great role in the stability and robustness of memory cells. Therefore, very careful design and analysis are necessary for reliable operation.

The 6-transistor (6T) SRAM cell is the most common memory cell configuration, due to its simple structure and efficient operation. It has a stable data storage because of its bistable property of its cross-coupled inverter pair. The access transistors allow for communication with the bit lines during read and write cycles. However, the performance of the 6T SRAM cell is heavily dependent on the transistor characteristics that vary with technology scaling. Therefore, it is critical to understand the effect of scaling on cell behavior to maintain the performance and reliability. A further important aspect of SRAM design is the power consumption versus silicon area trade-off. Reducing power consumption is a major design goal for today's portable and battery-powered devices. At the same time, the minimization of layout area is very important for obtaining higher memory density and reducing fabrication costs. These factors require the analysis of SRAM cells at different technology nodes to understand the change of design constraints with scaling.

To examine these aspects, simulation-based analysis is an effective approach to studying circuit behaviour before fabrication. Tools like Microwind allow designers to perform layout designs and circuit-level simulations in one environment. By using advanced device models like BSIM4, these simulations can reflect realistic transistor behavior, enabling more accurate assessments of circuit performance in various operating conditions. This work conducts a systematic study on a conventional 6T CMOS SRAM cell across multiple technology nodes. It focuses on understanding how scaling impacts key design parameters and overall cell behavior. Through consistent design methodology and simulation, this study aims to provide insights that can help develop efficient and reliable SRAM architectures for next-generation VLSI systems.

II. LITERATURE SURVEY

Static Random Access Memory (SRAM) continues to be a fundamental component in VLSI systems due to its high-speed operation and compatibility with CMOS technology. Over the years, extensive research has been carried out to improve the performance of SRAM cells in terms of power consumption, access speed, stability, and area efficiency, particularly with the continuous scaling of semiconductor technology.
Early work by Hansraj *et al.* [1] focused on the design of ultra-low power SRAM cells using 90 nm CMOS technology, demonstrating that careful transistor sizing and circuit optimization can significantly reduce power consumption while maintaining high-speed operation. Similarly, Akshay Bhaskar [2] explored various low-power SRAM design techniques, emphasizing the importance of minimizing both dynamic and static power dissipation. Mahanta *et al.* [7] further proposed a low-power 6T SRAM cell with improved access characteristics. These studies highlight the growing need for energy-efficient SRAM designs in modern electronic applications. Comparative analysis across different technology nodes has been widely studied. C. Ashok Kumar and B. K. Madhavi [3] evaluated 6T SRAM performance at 180 nm and 90 nm nodes, showing improvements in speed and reduction in power consumption with scaling. Mittal [5] extended this analysis across multiple technology nodes, emphasizing the influence of scaling on key performance parameters. Bagali *et al.* [8] also demonstrated reductions in power consumption and layout area at smaller nodes. These works confirm that technology scaling enhances SRAM efficiency, although it introduces additional design challenges.

Stability and reliability issues become more prominent in scaled technologies. Ayon Manna [4] proposed an adiabatic word line technique to improve read noise margin and reduce read disturbance. P. T *et al.* [6] discussed challenges such as leakage currents, process variations, and reduced noise margins in deep-submicron technologies. Sahu *et al.* [10] analyzed power-delay trade-offs in nanoscale CMOS, while N. D K *et al.* [11] explored FinFET-based SRAM designs, showing improved control over short-channel effects and leakage behavior. These studies highlight the need for robust design techniques in advanced nodes. Analysis by Kedar et al. [12] of SRAM and DRAM using Microwind proved that Microwind is capable of performing both integrated layout and simulations, which was very helpful to evaluate performance of memory circuits.

It is observed that most existing studies utilize simulation tools such as Cadence Virtuoso and SPICE-based environments, which primarily focus on schematic-level analysis with layout handled separately. In contrast, the present work employs the Microwind, which integrates both layout design and circuit simulation within a single platform. This enables direct evaluation of both physical layout and electrical performance across 120 nm, 90 nm, 70 nm, and 50 nm technology nodes, with emphasis on power consumption and cell area.

III. 6T SRAM CELL

The 6 Transistor (6T) SRAM cell is an extensively used memory configuration in present-day VLSI circuits because of its good balance among compactness, energy consumption, and reliability [6][8]. The basic cell consists of two CMOS inverters coupled with each other to produce a bistable flip-flop arrangement, and two NMOS transistors that serve as an access point between the storage nodes within the cell and the external bit lines. The storage nodes, namely Q and $\overline{Q}$, hold complementary binary digits, thus providing high stability for stored bits. The storage nodes are linked to the differential bit lines (BL and B$\overline{L}$) using two NMOS transistors that respond to a word line signal (WL).

A. Read Mode

Before commencing the read operation, the two bit lines are first set to a high voltage value, which is typically equivalent to the supply voltage. Upon activating the word line, the access transistors conduct, thus enabling the internal memory cell nodes to be coupled to the bit lines. Based on the state of the stored information, one node takes up a logic ‘0’ state, which in turn enables the pull-down NMOS transistor to provide a conduction path, resulting in a slight reduction of voltage on the corresponding bit line, while the other maintains its voltage level. The voltage differential on BL and B$\overline{L}$is sensed to indicate the stored logic [12].

A major difficulty faced during this process lies in maintaining the stored information. This is due to the direct coupling of the memory cell internal node to the bit line; any disturbance in the voltage on the node holding logic ‘0’ can cause problems, particularly with respect to feedback of the cross-coupled inverters, which in turn causes flipping of the logic states. Hence, proper transistor sizing[3][5] is necessary so that the pull-down NMOS transistor dominates the access transistor.

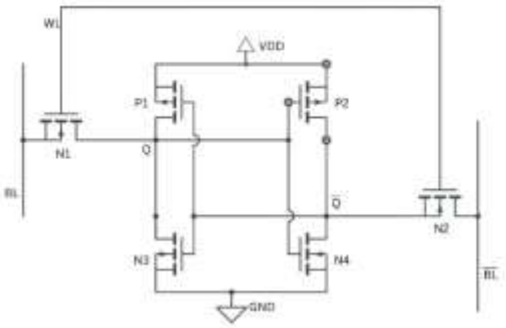

Fig. 1 Conventional 6T SRAM cell configuration

B. Write Mode

During writing, complementary data are fed to the bit lines with the assertion of the word line. Access transistors will now be turned on and allow the bit line drivers to change the logic states at the storage nodes. One storage node will be pulled up to the logic value of ‘1’ while the other will be pulled down to logic ‘0’. In this manner, the old data will be overwritten and the new stable logic state will be set.

Write operations require the use of access transistors sufficiently strong compared to the feedback of the cross-coupled inverters in order to overcome the old states. Failure to do so will lead to ineffective write operations especially for scaled technologies [3].

C. Hold Mode

While holding the data, the line word is held at logic low, which switches off the access transistors to isolate the SRAM cell from the bit lines. At this point, the data in the cross-coupled inverters is held using the positive feedback loop such that one node is always high, logic ‘1’, while the other node is low, logic ‘0’. With the supply voltage maintained, the information will stay as is without being influenced by any external force [12]. There is no activity in terms of switching when the data is held, and hence ideally, there should be no power consumed. Nevertheless, power loss will result from leakage current, which is associated with CMOS technology [6].

IV. PROPOSED METHOD

A. 6T SRAM Cell Implementation

The transistor level design of the 6T SRAM cell under the Microwind simulation platform is illustrated in Fig. 2. The design involves two CMOS inverters operating in a cross-coupling mode acting as the storage unit and two NMOS transistors serving as the access mechanism, which are gated using the word line (WL). Nodes Q and $\bar{Q}$ are interfaced with the bit line BL and its complementary line BLB, allowing for data transfer within the cell. The sizes of the transistors (W/L ratio) are precisely stated to ensure balanced pull-up, pull-down, and access transistors.

B. Technology Node Selection and Device Modeling

The four nodes chosen for scaling investigations are 120 nm, 90 nm, 70 nm, and 50 nm. In order to investigate the effects of scaling accurately, the same 6T SRAM cell will be designed using the same approach for all nodes but scaling its dimensions depending on the technology file. It would not make sense to redesign the circuit again since the main objective here is to observe how the characteristics change due to different technology and not architecture.

Behavior of the devices is modeled by BSIM4 model in the Microwind simulation environment. Non-ideal phenomena captured by the BSIM4 model include channel length modulation, drain induced barrier lowering (DIBL), mobility reduction and subthreshold leakage [10], and they tend to be more important with shrinking feature sizes [11], which makes the above models crucial when investigating the characteristics of 70 nm and 50 nm designs.

Simulations will be performed under the same stimuli and timing conditions to ensure consistency among the results of different nodes. Power consumption will be obtained from the transient simulation, whereas chip area will be measured from the layout design.

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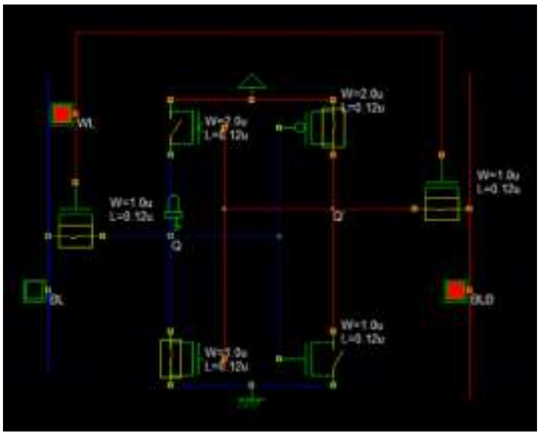

Fig. 2 Schematic Layout of 6T SRAM in DSCH2

C. Layout Design Using Microwind

The physical layout of the 6T SRAM cell is developed using the Microwind environment, which provides an integrated platform for both layout creation and circuit simulation. The tool includes predefined CMOS technology files—cmos012.rul (120 nm), cmos90n.rul (90 nm), cmos70n.rul (70 nm), and cmos50n.rul (50 nm)—each defining node-specific design rules, minimum feature sizes, interconnect layers, and BSIM3/BSIM4-based device parameters. The supply voltage is set according to the selected technology node, with values of 1.2 V, 1.0 V, 0.7 V, and 0.5 V respectively, to reflect realistic operating conditions.

The SRAM cell is built using standard layers, like diffusion, polysilicon, contacts, and metal interconnects. These layers include areas where tiny electronic parts are made, gates that control the flow of electricity, connections between parts, and metal paths that let electricity flow[12]. When these layers are put together, they form the special pair of inverters and transistors that the SRAM cell needs to work [8]. To make sure the design is correct and can be made, the people designing it have to follow strict rules about how the different parts are laid out, including how wide they are, how far apart they are, and how they line up.

When designing with different technology nodes, a consistent approach is used. This means that the same basic layout is kept, and the parts are placed in the same relative positions. The only change made is to scale the design to fit the new technology, using the rules defined in the technology file. This way, the analysis can concentrate on how the technology affects the design, rather than on differences in how the design is laid out. By keeping the layout consistent, it's easier to see the impact of changing the technology, and to make comparisons between different designs. This approach helps to ensure that the results are due to the technology change, rather than other factors.

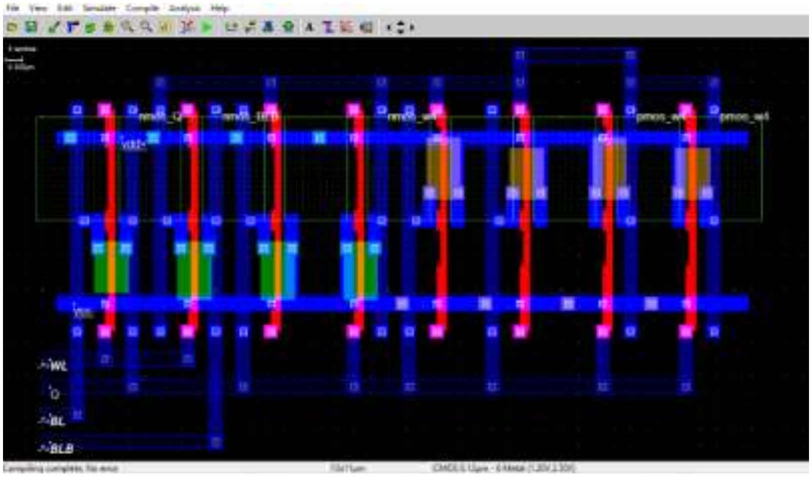

Fig. 3 Layout of 6T SRAM in Microwind

D. Simulation and Performance Evaluation

The performance analysis of the 6T SRAM cell is carried out via time domain simulation using Microwind, where the electrical characteristics as well as efficiency parameters of the cell at various technology nodes are evaluated. For

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simulation purposes, controlled pulses are provided on the WL and bit lines (BL and B$\overline{\text{L}}$), so that sequential read and write operations [2][7], can be performed and the cell operation is seen realistically.

From an overall perspective, there are mainly three points that have been taken into account to evaluate the performance of the cell. They include voltage levels at the internal nodes (Q and $\overline{\text{Q}}$), power consumption as well as layout area. The voltage at the internal nodes are measured to ensure that proper logic levels exist and whether there is any deviation from the expected levels due to scaling. Voltage variations and switching characteristics can be obtained in order to analyze the speed and signal integrity.

The other aspect includes power consumption, both dynamic and static power. The power can be calculated based on the current drawn from the supply during switching operation as well as when it is inactive or idle. The power consumption changes with different nodes. Layout areas, which provide an idea about the physical efficiency, have been calculated. In order to conduct a fair evaluation, the simulation conditions as well as input patterns have been maintained constant among different nodes.

V. SIMULATION RESULT AND COMPARITIVE ANALYSIS

The functional behavior and performance of the designed 6T SRAM cell have been confirmed using the simulation process at the logic level as well as the layout level. The DSCH2 simulation process is carried out to ensure that the functioning of the SRAM cell is correctly implemented in logic form using control signals on the wordline and bitlines. The Verilog netlist extracted from DSCH2 is imported into the Microwind software for the purpose of performing post layout simulations. The advantage gained here is that the simulation takes into account real-life physical parameters such as parasitics and interconnects within the physical design and hence offers a more accurate picture of the circuit operation.

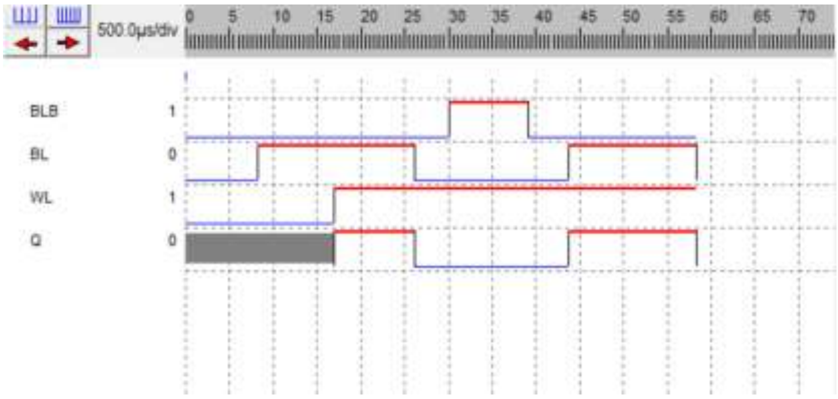

Fig. 4 DSCH2 waveform showing 6T SRAM read/write operation.

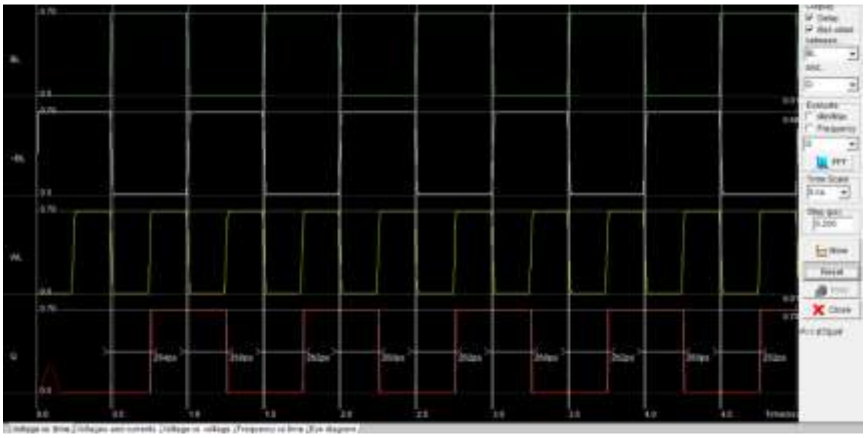

Fig. 5 Microwind waveform showing switching delay of 6T SRAM cell.

The transient waveform confirms proper switching of the storage node (Q), with a measured **propagation delay of approximately 260 ps**. In order to analyze the effect of scaling, various CMOS technology files for 120 nm, 90 nm, 70 nm, and 50 nm nodes are chosen. The nodes are then analyzed using their specific operational conditions.

A. Power Consumption Analysis

There exists a clear monotonic decrease in power dissipation with technology scaling. In terms of power dissipation, the 6T SRAM cell has a dissipation rate of about 9.807 µW at 120nm, 5.167 µW at 90nm, 1.672 µW at 70nm, and 0.349 µW at 50nm. This amounts to a significant decrease in power dissipation of nearly 96.4%. The main contributor to this trend is the decrease in supply voltage as well as the effective switching capacitance in the small nodes. Because of the proportionality of the dynamic power to the product $C \cdot V^2 \cdot f$, the decrease in supply voltage becomes even more pronounced due to its quadratic dependence. The other reason is that the decrease in the dimension of the transistors reduces the intrinsic capacitance of the transistor, thereby lowering the amount of energy expended during the switching action.

B. Cell Area Analysis

The physical dimensions of the SRAM cell have also been greatly reduced with shrinking feature sizes. This occurs with the decrease of layout area from around 53.4 µm² at 120 nm to 37.1 µm² at 90 nm, 18.2 µm² at 70 nm, and 9.3 µm² at 50 nm, resulting in a total reduction of around 82.6%. The phenomenon described above conforms to the scaling pattern, since the area will decrease almost proportionally to the inverse square of the feature size. As the cell area decreases, it results in increased density of memory. It means that more cells can fit in the same amount of silicon area, which becomes essential for VLSI/SoC technology.

TABLE I: COMPARATIVE ANALYSIS OF POWER CONSUMPTION AND LAYOUT AREA OF 6T SRAM CELL ACROSS DIFFERENT TECHNOLOGY NODES

PARAMETERS	**TECHNOLOGY NODES**			
	50nm	**70nm**	**90nm**	**120nm**
POWER CONSUMPTION (µW)	0.349	1.672	5.167	9.807
CELL LAYOUT AREA (µm^2)	9.3	18.2	37.1	53.4

A joint assessment of power and area shows clear enhancement of the SRAM operation with smaller technologies. Both parameters display decreasing tendency when the node size becomes lower; therefore, there is an effective scaling of the 6T SRAM cell. One should notice the better reduction of power compared to area: it is expected because energy efficiency is improved faster than the size reduction. Nodes 70 nm and 50 nm demonstrate the largest improvements and could be applied for low-power and high-density operations. As to node 120 nm, its area and power consumption are rather big, but the stability is higher than in the other two cases; therefore, 120 nm could be used in cases where the priority is not density but robustness of operation.

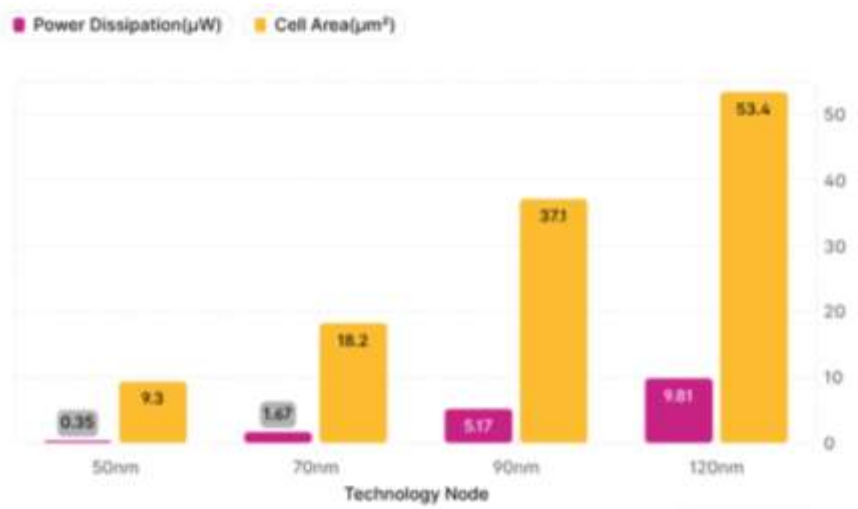

Fig. 6 Comparison between Power Consumption and Cell Layout Area Across Technology Nodes

The power saving is very non-uniform between nodes. The power drops about 47.3% from 120 nm to 90 nm and a sharper drop of about 67.7% from 90 nm to 70 nm. The most aggressive reduction is from 70 nm to 50 nm, which has the reduction of approximately 79.1%. This shows that the scaling benefits become stronger at lower nodes. In contrast, the layout area reduction happens more gradually. The area is decreased by ~30.7% from 120 nm to 90 nm, and by ~50.9%

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from 90 nm to 70 nm. The last transition from 70 nm to 50 nm shows a drop of about 48.9%, indicating a rather constant scaling trend. The insight from the result is that the power reduction rate is larger than the area reduction at each scaling step, with differences up to more than 30% in some transitions. Also, the overall scaling ratio from 120 nm to 50 nm is about 28× reduction in power versus about 5.7× reduction in area. This underscores the fact that energy efficiency improves far more aggressively than physical scaling.

VI. CONCLUSION

In this study the objectives have been successfully achieved by the systematic design and evaluation of a conventional 6T CMOS SRAM cell over various technology nodes. The work effectively isolates and analyses the impact of technology scaling on the key performance parameters, keeping the design conditions same and using BSIM4 based modeling in Microwind environment. Transient simulation is used to accurately characterize the behavior of the SRAM cell during read and write operations so as to achieve both functional correctness and realistic performance assessment.

Comparative analysis demonstrates that scaling from 120 nm to 50 nm consistently yields improvements in both dynamic power consumption and layout area. Specifically, reductions of approximately 96.4% in power and 82.6% in area were observed, which aligns with the anticipated advantages of technology scaling. This further supports the notion that employing smaller technology nodes can enhance energy efficiency and compactness, without detriment to operational reliability. This study provides a practical and comprehensive understanding of SRAM behavior within scaled CMOS technologies. The findings contribute valuable insights into memory design for contemporary VLSI systems, simultaneously highlighting promising directions for future research concerning advanced SRAM architectures and performance optimization.

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