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Performance Evaluation of Differential 2T-2MTJ Memory Configurations Based on Diverse Magnetic Tunnel Junction Models

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Abstract: Traditional volatile memories like SRAM and DRAM face scaling limits. These memories have high leakage power and volatility issues. Spin-Transfer Torque Magnetic Random-Access Memory (STT-MRAM) is a strong non-volatile alternative. This paper presents a comparative analysis of three Magnetic Tunnel Junction (MTJ) models. These models include Perpendicular MTJ (PMA), Shape-PMA (s-PMA), and Double-Barrier MTJ (DMTJ).

Simulation results show that the Double-Barrier MTJ (DMTJ) is the best device. It has a fast switching delay of 2.20 ns. It also uses a low switching current of 3.68 µA. Based on these results, this paper implements a differential 2T-2DMTJ cell architecture. The proposed design uses differential sensing for high reliability. The 2T-2DMTJ cell shows strong performance. The simulation results for the 2T-2DMTJ architecture demonstrate an average write power of 13.47 µW and an exceptionally low read power of 3.85 nW, while maintaining a standby power of 439.24 pW. It achieves a write delay of 1.085 ns and a read delay of 12.66 ps.

Keywords: STT-MRAM, Magnetic Tunnel Junction (MTJ), Double-Barrier MTJ (DMTJ), 2T-2MTJ Cell, Non-Volatile Memory, Spintronics.

I. INTRODUCTION

Memory is the heart of modern computation. It stores data and instructions for the processor. The memory subsystem directly affects system performance and power consumption. Traditionally, memory follows a hierarchy from fast cache to large non-volatile storage. However, conventional charge-based memories like Flash suffer from limited endurance and scaling constraints at sub-40 nm nodes.

Static Random-Access Memory (SRAM) and Dynamic Random-Access Memory (DRAM) are the main parts of this hierarchy. They offer high speed but face the major problem of volatility. Volatile memory loses data when power is off. SRAM needs constant power to hold its state, and DRAM needs a continuous refresh process. These requirements lead to high power leakage. The physical separation of the CPU and memory also creates a bottleneck known as the "memory wall".

Researchers study new alternatives like Magnetoresistive RAM (MRAM) to solve these limits. MRAM stores data using electron spin rather than electric charge. It offers speeds comparable to SRAM. It also has virtually unlimited write endurance. Because it is non-volatile, it uses zero standby power to keep its magnetic state. This technology is a top candidate for advanced memory applications. This study compares different MTJ devices and implements a reliable 2T-2DMTJ cell architecture.

II. LITERATURE REVIEW

Recent advancements in SRAM design have been directed towards enhancing resilience against radiation-induced SNUs and DNUs, which are critical for reliable operation in aerospace and other radiation-prone environments.

Current research into spintronic non-volatile memories (NVMs) is driven by the demand for energy-efficient alternatives to traditional charge-based memories. Conventional memories like Flash and EEPROM face significant limits in endurance, programming voltage, and scaling at sub-40 nm nodes. These drawbacks have catalyzed the development of Magnetic Tunnel Junction (MTJ) technologies that use electron spin rather than electric charge to store data. MRAM technology offers a unique combination of high speed, unlimited endurance, and CMOS compatibility. Unlike charge-based systems, MRAM stores information in the magnetic orientation of ferromagnetic layers, which enables "instant-on" computing and eliminates standby power consumption.

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A. *Evolution and Principles of STT-MRAM*

Spin-Transfer Torque MRAM (STT-MRAM) represents the first generation of practical spintronic memory. It uses an MTJ stack consisting of a pinned reference layer, a free storage layer, and a thin insulating barrier, typically MgO. The resistance of the MTJ depends on the relative magnetization of these layers through the tunneling magnetoresistance (TMR) effect.

When magnetizations are parallel, the junction exhibits low resistance; when antiparallel, it exhibits high resistance. STT-MRAM combines the high speed of SRAM with the non-volatility of Flash. Tehrani et al. [1] show that MRAM offers a unique combination of high speed and unlimited endurance. However, as technology nodes advance toward sub-20 nm, maintaining adequate thermal stability becomes a fundamental challenge.

B. Advanced MTJ Variants: s-PMA and DMTJ

To overcome scaling and energy limitations, researchers have developed innovative MTJ variants. Shape Perpendicular Magnetic Anisotropy (s-PMA) MTJs achieve perpendicular magnetization through geometric engineering of high-aspect-ratio free layers. Watanabe et al. [3] demonstrate that shape anisotropy becomes the dominant contribution to perpendicular anisotropy in single-digit nanometer MTJs. This approach is particularly advantageous at sub-20 nm nodes where interfacial effects alone may not be enough to maintain data.

Double-Barrier MTJs (DMTJs) offer another significant advancement by incorporating a second tunnel barrier and an additional ferromagnetic layer into the stack. Almeida et al. [4] report that DMTJs demonstrate functional efficiency increased by a factor of 4 compared to conventional designs. Optimized DMTJs achieve higher spin-torque efficiency, which directly translates to reduced critical switching currents and 30-50% reduction in write energy. Hybrid s-PMA DMTJ designs combine these benefits, achieving exceptional thermal stability factors exceeding 80 and high area efficiency.

C. MRAM Architecture and Computing-in-Memory

MRAM cell designs are evolving to meet the needs of specialized applications. The conventional 1T-1MTJ architecture remains the workhorse of commercial products due to its compact footprint. Rho et al. [2] demonstrate a 4 Gb capacity using compact $9F^2$ cells in 28 nm technology. However, emerging applications in hardware security and high-reliability systems have driven the exploration of alternative multi-transistor architectures.

Multi-transistor designs like the 2T-2DMTJ offer better reliability. Zhang et al. [5] show that these architectures improve sensing margins and noise immunity. The 2T-2MTJ architecture, often configured for differential or self-referencing operation, doubles the sensing margin and improves noise immunity. These advanced architectures also enable Compute-in-Memory (CiM) and Logic-in-Memory (LIM) paradigms. CiM architectures perform computation directly within the memory array, which addresses the "memory wall" bottleneck. For instance, a 2T1DMTJ configuration reduces execution time by 78% for machine learning operations like XNOR-Bitcount by eliminating costly data movement.

III. MAGNETIC TUNNEL JUNCTION DEVICES

Magnetic Tunnel Junction devicess (MTJs) serve as the fundamental building blocks of modern spintronic devices, operating primarily on the principle of quantum mechanical tunneling. This section details the architectural components of MTJs and evaluates the performance of three distinct models—the Perpendicular Magnetic Anisotropy (PMA) MTJ, the Shape Perpendicular Magnetic Anisotropy (s-PMA) DMTJ, and the Double-Barrier MTJ (DMTJ)—to determine their suitability for high-performance memory applications.

A. *Overview of MTJ Structure and Working Principle*

An MTJ is a three-layer spintronic device consisting of two ferromagnetic (FM) layers separated by a thin insulating barrier, typically Magnesium Oxide (MgO) as shown in Fig 1.

Architectural Components:

The standard MTJ architecture comprises three critical layers:

- *Pinned Layer (PL): A reference layer with a fixed magnetic orientation, often stabilized by an adjacent antiferromagnetic (AFM) layer.*
- *Tunneling Barrier (TB): A thin insulating layer that allows electrons to tunnel through based on the quantum mechanical effect of tunneling magnetoresistance (TMR).*
- *Free Layer (FL): A ferromagnetic layer whose magnetic orientation can be switched via current or magnetic fields.*

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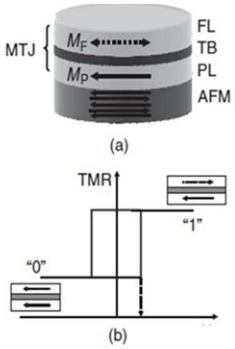

Figure 1: (a) Basic MTJ Structure; (b) TMR Hysteresis Loop.

Data storage is achieved through the relative magnetic alignment of the FL and PL. A parallel (P) state results in low electrical resistance (binary "0"), while an anti-parallel (AP) state results in high resistance (binary "1").

B. Advanced MTJ Architectures

To address the requirements for higher density and thermal stability, MTJ designs have evolved from in-plane configurations to advanced perpendicular structures:

- PMA MTJ: Utilizes perpendicular magnetic anisotropy to improve scalability and thermal stability for high-density MRAM.
- s-PMA DMTJ: An advanced double-barrier structure where the free layer thickness (t) exceeds its diameter (d), utilizing shape anisotropy to enable scaling to sub-10 nm nodes.
- Double-Barrier MTJ (DMTJ): Features a combination of double barriers and synthetic double-free layers to enhance the Spin-Transfer Torque (STT) effect, leading to superior switching efficiency.

Fig 2 illustrates the s-PMA DMTJ Architecture and DMTJ Stacked Architecture

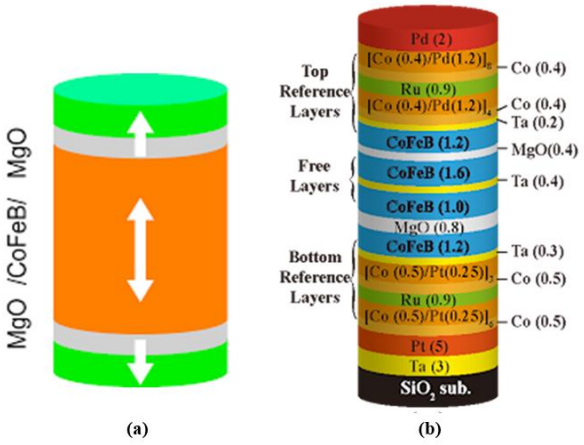

Figure 2: (a) s-PMA DMTJ Architecture; (b) DMTJ Stacked Architecture

The compact models for these devices are defined by specific physical parameters in Verilog-A, as detailed in Table 1.

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Parameter	Description	PMA MTJ	s-PMA DMTJ	DMTJ
alpha	Gilbert damping	0.027	0.005	0.004
gamma	Gyromagnetic ratio	1.760×10^{11} rad·s^{-1}·T^{-1}	1.760×10^{11} rad·s^{-1}·T^{-1}	1.760×10^{11} rad·s^{-1}·T^{-1}
P	Electron polarization	0.52	0.57	0.71
Ms	Saturation magnetization	1.460×10^{6} A/m (μ_0·Ms = 1.84 T)	1.2096×10^{6} A/m (μ_0·Ms = 1.52 T)	1.257×10^{6} A/m (μ_0·Ms = 1.58 T)
PhiBas	Energy barrier height	0.4 eV	0.4 eV	0.4 Ev
Vh	Half-TMR voltage	0.5 V	0.5 V	0.5 V
tsl / tfl	Free layer height	1.3 nm (tsl)	15 nm (tsl)	1.6 nm (tflt), 1.6 nm (tflb)
a, b / r	Device dimensions	40 × 40 nm	5.25 nm (radius)	20 × 20 nm
tox / toxb / toxt	Oxide barrier thickness	0.85 nm (tox)	0.85 nm (toxb), 0.25 nm (toxt)	0.8 nm (toxb), 0.4 nm (toxt)
TMR	TMR(0)	1.8 180%	2.0 200%	1.8 180%
RA	Resistance × area product	5 Ω·μm²	4.5 Ω·μm²	10 (top), 10 (bot) Ω·μm²
T	Temperature	300 K	300 K	300 K

Table 1: Verilog-A Model Parameters of Various MTJs

C. Comparative Performance Analysis

The performance of these models was evaluated through simulations within a dedicated test bench circuit shown in Fig 3.

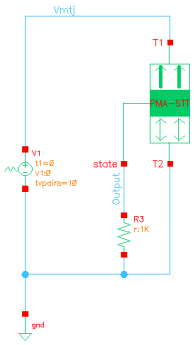

Figure 3: MTJ Test Bench Circuit Schematic.

D. Transient Analysis

Fig 4 illustrates the Switching Delay characteristics for various MTJ models. The DMTJ model shows a significant advantage in speed, requiring only 2.20 ns for switching, compared to 5.68 ns for the other two models.

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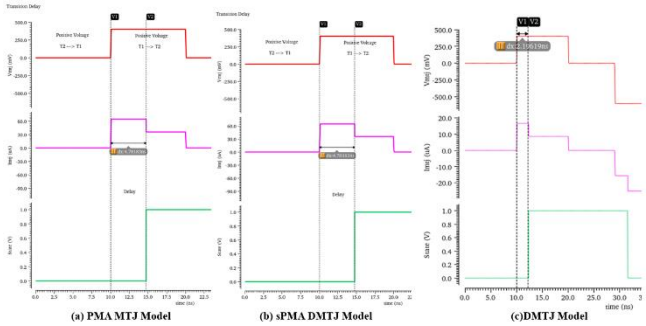

Figure 4: Switching Delay characteristics for various MTJ models.

E. DC Analysis

The DC sweep simulations of the MTJ devices show how voltage drives the switching behavior.

The voltage-driven switching and the hysteresis loop for the various MTJ models are shown in Fig 5.

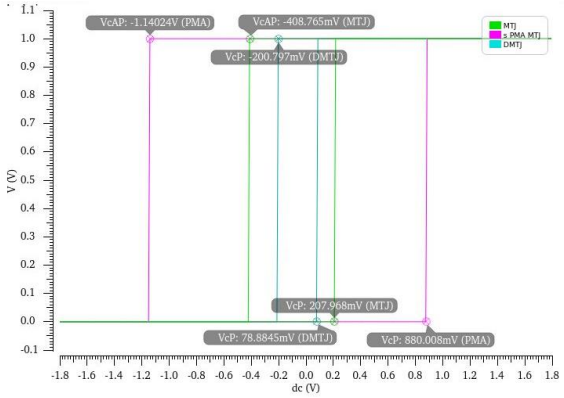

Figure 5: Switching Voltage hysteresis loops.

The Resistance (R-V) characteristics in Figure 6 shows the TMR behavior and how the states change for each model.

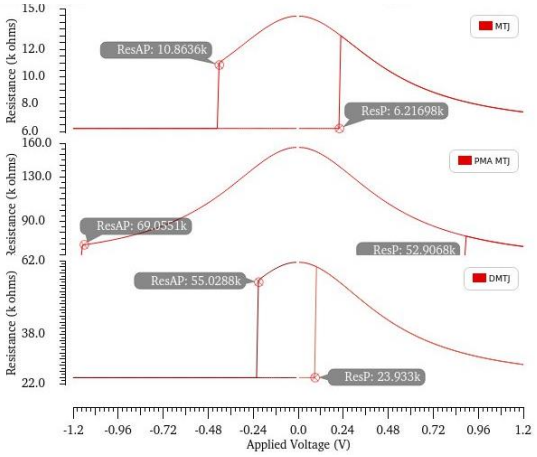

Figure 6: Resistance (R-V) characteristics.

Additionally, the (I-V) curve comparative analysis in Figure 7 highlights that the DMTJ model has exceptionally low switching currents.

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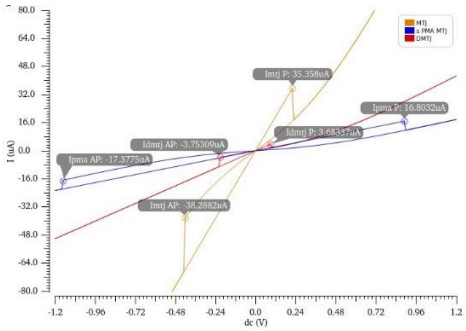

Figure 7: I-V Curve Comparative Analysis

The results for switching voltage (Vc), critical current (Imtj), and resistance are listed in Table 2.

Models/ Parameters	STT PMA MTJ	s-PMA DMTJ	Double-Barrier MTJ
VcAP	408.765mV	-1.14024 V	-200.797mV
VcP	207.968mV	880.008mv	78.8845mV
Imtj AP	-38.288 uA	-17.3775 uA	-13.75309 uA
Imtj P	35.358 uA	16.8032 uA	3.68337 uA
Res AP	10.836 kΩ	69.055 kΩ	55.028 kΩ
Res P	6.217 kΩ	52.906 kΩ	23.933 kΩ
Switching Delay	5.68149ns	5.68149ns	2.19619ns

Table 2. Comparative analysis of Various MTJ Devices

F. Summary of Findings

Based on simulation data, the Double-Barrier MTJ (DMTJ) is identified as the most promising candidate for next-generation in-memory computing (IMC). Its primary advantages include the fastest switching speed (approx. 2.20 ns), superior energy efficiency (lowest switching current of 3.68 µA), and an enhanced STT effect due to its double-barrier design.

IV. 1T-1MTJ STT MRAM CELL

Following the device-level analysis of Magnetic Tunnel Junctions (MTJs), this chapter explores their application within a standard memory cell. The 1T-1MTJ (one transistor, one MTJ) configuration is the fundamental building block for high-density Spin-Transfer Torque (STT) MRAM.

A. 1T-1MTJ Cell Architecture and Operation

The 1T-1MTJ cell provides a compact design for non-volatile memory. 1T-1MTJ MRAM Circuit is shown Fig 8.

Its structure consists of:

- 1T (One Transistor): A single access transistor (typically NMOS) that functions as a switch, with its gate connected to the Word Line (WL).
- 1MTJ (One MTJ): A Magnetic Tunnel Junction that acts as the data storage element.
- Configuration: The MTJ is connected in series with the access transistor, and this combination is placed between the Bit Line (BL) and the Source Line (SL).

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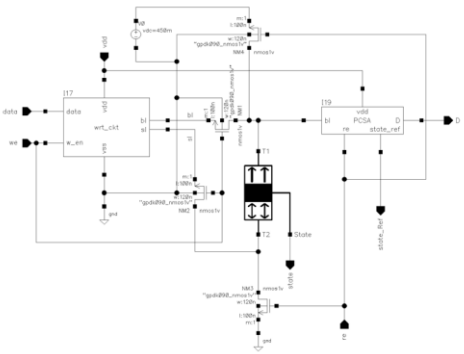

Figure 8: 1T-1MTJ MRAM Circuit Architecture.

Operation Principle

- Data Storage: The MTJ stores logic '0' or '1' as resistance states (Low-R Parallel or High-R Antiparallel).
- Access Control: When WL is HIGH, the transistor turns ON, connecting the MTJ to the BL and SL. When WL is LOW, the transistor is OFF, isolating the MTJ to retain data (Hold state).
- Write Operation: A differential voltage across BL and SL drives a bi-directional current through the MTJ, using the STT effect to switch the magnetic state.
- Read Operation: A small sensing voltage (e.g., 450 mV) is applied to measure the resistance without disturbing the stored state.

B. 1T-1MTJ Operational States

Specific operations are controlled by voltage levels applied to the control lines, as detailed in Table 3.

Operation	WL	BL	SL	Description
Write '1' (Set to AP)	HIGH	1.8V	0V	Current flows BL to SL; STT effect switches MTJ to Antiparallel (AP) state.
Write '0' (Set to P)	HIGH	0V	1.8V	Current flows SL to BL; reverse STT switches MTJ to Parallel (P) state.
Read	HIGH	450mV	0V	Sensing current measures resistance: High-R is '1', Low-R is '0'.
Hold (Standby)	LOW	Floating	Floating	Transistor is OFF, isolating the MTJ for non-volatile storage.

Table 3: Operational States of the 1T-1MTJ STT MRAM Cell

C. Simulation Analysis of 1T-1MTJ STT MRAM

i. Timing Waveforms

Sequential operations including Write, Hold, and Read cycles were simulated to confirm the correct switching and retention behavior of the cell. During the Write 1 phase, the data line is driven high while the word line activates the access transistor to switch the MTJ state. In the Hold phase, the word and read lines remain inactive to maintain data without any current flow. Finally, the Read phase applies a small sensing voltage to detect the MTJ resistance without disturbing its stored state. These cycles are illustrated in the timing diagram of 1T-1MTJ STT MRAM cycles in Fig 9.

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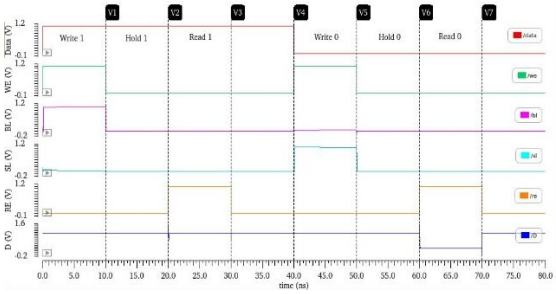

Figure 9: Timing diagram of 1T-1MTJ STT MRAM cycles.

ii. Bitline Current Comparison

Distinct current magnitudes are observed for each specific operation. High currents in the range indicate the MTJ state transitions during write phases. Hold phases exhibit negligible current, which confirms the non-volatility of the device. Read phases show small sensing currents between and, demonstrating a stable and non-destructive readout process. The comparison of these bitline currents across memory operations is shown in Fig 10.

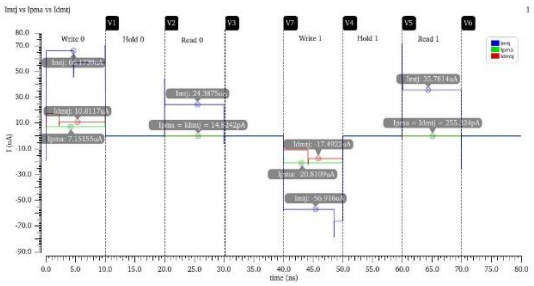

Figure 10: Bitline current comparison across memory operations.

D. Comparative Performance Analysis

The choice of MTJ model significantly impacts cell performance. Table 4 compares the metrics for Conventional, PMA-MTJ, and DMTJ models.

Parameter	**MTJ**	**PMA-MTJ**	**DMTJ**
Dynamic Power	14.2521 mW	1.9165 mW	**335.353 nW**
Write Delay	4.67138 ns	10 ns	**2.2104 ns**
Read Delay	40.0502 ns	40.5064 ps	**31.6628 ps**
Write Power	104.325 mW	37.2716 mW	**26.3376 mW**
Static Power	24.4953 nW	30.3021 nW	**17.2942 nW**

Table 4: 1T-1MTJ Comparative Analysis Metrics

The DMTJ-based cell (blue line) demonstrates exceptional performance, offering nano-watt-level dynamic power and significantly faster write/read speeds than its counterparts as shown in Fig 11.

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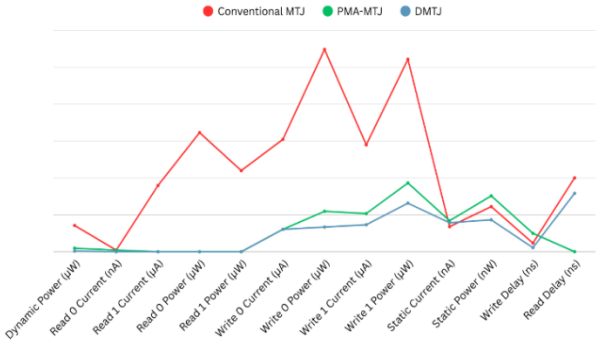

Figure 11: Parametric comparison of the three MTJ Models.

The DMTJ-based cell (blue line) demonstrates exceptional performance, offering nano-watt-level dynamic power and significantly faster write/read speeds than its counterparts.

E. Summary of findings

The 1T-1MTJ architecture paired with the Double-Barrier MTJ (DMTJ) provides ultra-fast speeds and high energy efficiency. This makes it an ideal candidate for advanced embedded memory applications where power and speed are critical constraints.

V. 2T-2MTJ STT MRAM CELL

While the 1T-1MTJ cell configuration is widely used for high-density applications, the 2T-2MTJ (two transistor, two MTJ) architecture is frequently employed in systems requiring enhanced reliability and performance, such as in-memory computing. This chapter investigates the design, operational principles, and performance characteristics of this differential memory cell.

A. Architecture and Operational Principles

The 2T-2MTJ cell utilizes a differential design comprising two access transistors and two Magnetic Tunnel Junction (MTJ) storage elements as shown in Fig 12.

- Structure: The cell includes two access transistors, typically NMOS, with their gates tied to a common Word Line (WL). Each transistor is connected in series with its own MTJ device.
- Connectivity: Unlike the single-ended 1T-1MTJ cell, this architecture utilizes separate Bit Lines (BL and BLR) and Source Lines (SL and SLR) for each transistor-MTJ pair.
- Differential Storage: The two MTJs are designed to store complementary data. For instance, to represent a logic '1', MTJ1 is programmed to the Antiparallel (High-R) state while MTJ2 is set to the Parallel (Low-R) state.
- Performance Advantages: This differential storage allows for reliable differential readout, which significantly improves noise immunity and read margins. By sensing the difference in resistance rather than an absolute value, the cell is less susceptible to variations in Rp and Rap.

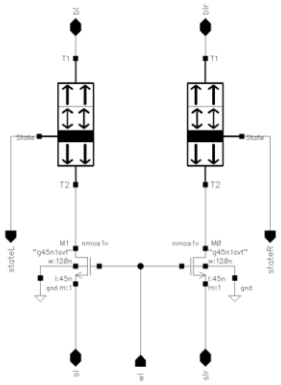

Figure 12: Schematic of the core 2T-2MTJ MRAM cell.

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B. Operational States

Coordinated voltage application to the four data lines (BL, BLR, SL, SLR) is required for successful differential operation. The voltage levels for each primary state are summarized in Table 4.

Operation	WL	BL	BLR	SL	SLR	Description
Write '1'	HIGH	1.8V	0V	0V	1.8V	Sets MTJ1 and MTJ2 to complementary states for logic '1'.
Write '0'	HIGH	0V	1.8V	1.8V	0V	Reverse current flows to set the MTJs to logic '0' states.
Read	HIGH	0.45V	0.45V	0V	0V	Differential resistance is sensed for a reliable readout.
Standby	LOW	Float	Float	Float	Float	Transistors are OFF, retaining complementary data non-volatilly.

Table 4: Operational States of the 2T-2MTJ STT MRAM Cell

C. Test Bench and Support Circuitry

To evaluate the 2T-2MTJ cell, it must be integrated into a larger test circuit comprising specific functional blocks as shown in Figure 13.

- Data Write Driver: Delivers high-voltage and high-current pulses to the bit and source lines to switch the MTJs.
- Precharge Circuit: Equalizes the voltage on both BL and BLR (typically to 0.5 * VDD) before read-sensing begins to ensure a stable starting point.
- Pre-Charge Sense Amplifier (PCSA): A differential amplifier that detects small voltage differences developing between BL and BLR during a read operation and amplifies them to full logic levels.

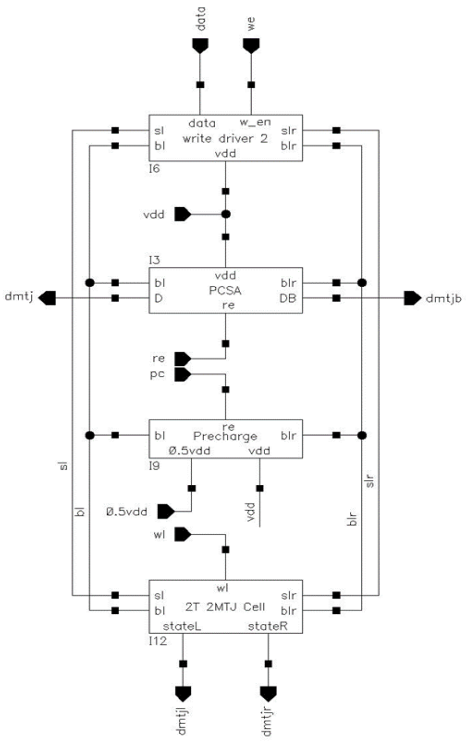

Figure 13: Test circuit schematic for the 2T-2DMTJ MRAM cell.

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D. Comparative Performance Analysis

The choice of MTJ model significantly impacts cell performance. Table 5 compares the metrics for Conventional, PMA-MTJ, and DMTJ models.

Metric	MTJ	PMA-MTJ	DMTJ
Write Delay	1.085 ns	59.909 ps	1.08537 ns
Read Delay	15.858 ps	15.047 ps	12.6611 ps
Dynamic Power	4.114 µW	1.945 µW	5.014 µW
Write Power (Avg)	16.44 µW	7.78 µW	13.47 µW
Read Power (Avg)	10.57 nW	27.65 nW	3.85 nW
Standby Power	718.71 pW	49.93 nW	439.24 pW

Table 5: Performance Analysis of Standard 2T-2DMTJ MRAM Cell

The timing diagram in Figure 14 illustrates the control sequence, including the activation of the Word Line (wl), Read Enable (re), and the resulting data outputs (D, DB).

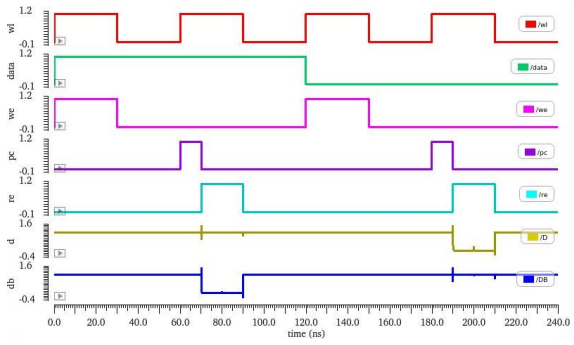

Figure 14: Timing diagram for the 2T-2DMTJ cell.

E. Summary of Findings

The 2T-2MTJ architecture utilizing the Double-Barrier MTJ (DMTJ) offers a superior balance of high-density performance and ultra-low power consumption. With an industry-leading read power of 3.85 nW and minimal standby leakage, it effectively addresses the energy constraints of modern SoC designs. This makes the DMTJ an ideal candidate for high-speed, non-volatile embedded memory where maintaining data integrity at picosecond read speeds is essential

VI. CONCLUSION

This research has provided a comprehensive evaluation of Magnetic Tunnel Junction (MTJ) technologies, progressing from fundamental device physics to complex memory cell architectures. The key findings of this study are summarized below:

- MTJ Model Optimization: The Double-Barrier MTJ (DMTJ) was identified as the superior storage element, demonstrating a significantly lower switching delay of 2.20 ns compared to the 5.68 ns observed in STT PMA and s-PMA DMTJ models.
- Energy Efficiency at the Device Level: The DMTJ exhibited the lowest critical switching current 3.68µA for P-to-AP switching and the tightest hysteresis loop, indicating minimal power requirements for state transitions.
- 1T-1MTJ Performance: Integrating the DMTJ into a standard 1T-1MTJ cell architecture resulted in a monumental reduction in dynamic power consumption, operating in the nano-watt range (335.353 nW) while conventional models remained in the milli-watt range.
- Architectural Robustness: The investigation of the 2T-2MTJ configuration validated its efficacy for high-reliability applications. Its differential nature provides superior noise immunity and improved read margins by sensing complementary data states between two MTJ branches.

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- Operational Integrity: Simulation waveforms for both the 1T-1MTJ and 2T-2MTJ cells confirmed stable and non-destructive read, write, and hold operations, fulfilling the requirements for reliable non-volatile memory.

Building upon the results of this study, future research will focus on scaling these spintronic solutions for high-density and high-computational environments:

- Current Reduction Strategies: Further research will investigate material stack optimizations and interfacial engineering to continue reducing the critical switching current, directly lowering the power overhead of the write operation.
- Memory Array Integration: Future efforts will move beyond single-cell analysis to the design and simulation of large-scale MRAM arrays, addressing challenges related to word line/bit line parasitic resistance and capacitance.
- In-Memory Computing (IMC): A primary goal is the implementation of these high-efficiency DMTJ cells into In-Memory Computing architectures. By utilizing the parallel-processing capabilities of the 2T-2MTJ differential scheme, logic operations can be performed directly within the memory array to eliminate data movement bottlenecks.Future work can focus on improving write stability and reducing access delays to further enhance performance.

REFERENCES

[1] X. Jia, G. Cheng, G. Zhang, and Y. Jiang, "Novel dual power hybrid write operation structure for STT-MRAM," International Journal of Electronics, vol. 112, no. 4, pp. 617–631, 2025.

[2] Tehrani, S., et al. (2000). Recent developments in magnetic tunnel junction MRAM. IEEE International Magnetics Conference.

[3] Rho, K. M., et al. (2017). 23.5 A 4Gb LPDDR2 STT-MRAM with compact 9F² 1T1MTJ cell and hierarchical bitline architecture. International Solid-State Circuits Conference.

[4] Watanabe, K., et al. (2018). Shape anisotropy revisited in single-digit nanometer magnetic tunnel junctions. Nature Communications.

[5] Almeida, T. P., et al. (2022). Off-axis electron holography for the direct visualization of perpendicular shape anisotropy in nanoscale 3D magnetic random-access-memory devices. APL Materials.

[6] Zhang, Y., et al. (2024). Complementary-magnetization-switching perpendicular spin-orbit torque random access memory cell for high read performance. IEEE Magnetics Letters.

[7] X. Jia, G. Cheng, G. Zhang, and Y. Jiang, "Novel dual power hybrid write operation structure for STT-MRAM," International Journal of Electronics, vol. 112, no. 4, pp. 617–631, 2025.

[8] P. Barla, V. K. Joshi, and S. Bhat, "A novel self write-terminated driver for hybrid STT-MTJ/CMOS LIM structure," Ain Shams Engineering Journal, vol. 12, pp. 1839–1847, 2021.

[9] S. R. Gupta, V. Sharma, and M. Jain, "HSCIM: A High Security Compute-in-Memory Architecture with PUF Based on TST-MRAM," Proc. IEEE Int. Symp. Circuits and Systems (ISCAS), 2025.

[10] A. K. Prakash and R. Ghosh, "Design of STT-MRAM Using Hybrid MTJ/CMOS for Applications Beyond CMOS," Proc. IEEE Int. Conf. Innovations in Science and Technology for Sustainable Development (ICISTSD), 2022.

[11] Y. Wang, D. Song, J. Dai, E. Deng, and W. Liu, "A Dual-Swing-Sample-and-Couple Sense Amplifier with Large Sensing Margin for STT-MRAM," IEEE Trans. Circuits Syst. II: Express Briefs, vol. 72, no. 7, Jul. 2025.

[12] Y. Wang, D. Song, E. Deng, Y. Xu, and W. Liu, "A High-Speed and High-Yield Path-Switching Sensing Circuit for STT-MRAM," IEEE Trans. Magn., vol. 61, no. 1, Jan. 2025.

[13] R. K. Pandey, S. Tiwari, and J. Singh, "Big-Computing and Little-Storing STT-MRAM PIM Architecture with Charge-Domain-Based MAC Operation," IEEE Trans. Comput., vol. 74, no. 3, 2025.

[14] N. Patel, D. Lee, and C. Wang, "CSA-CiM: Enhancing Multifunctional Computing-in-Memory with Configurable Sense Amplifiers," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 44, no. 2, 2025.

[15] J. Lin, Y. Zhang, and M. Park, "Extremely Low Switching Current STT-MRAM Device with Double Spin Transfer Torque," IEEE Electron Device Lett., vol. 46, no. 5, 2025.