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Implementation on "Area-Delay-Power Efficient Carry-Select Adder"

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Abstract: In this paper, we made an analysis on the logic operations involved in conventional carry select adder (CSLA) and CSLA based on binary to excess-1 converter (CSLA-BEC) to study the data-dependency, and to find redundant logic operations. We have eliminated all the redundant logic operations of conventional CSLA, and proposed a logic formulation for CSLA. In the proposed scheme, the carry-select operation is scheduled before the calculation of final-sum, which is different from the conventional approach. To optimize the logic units, an efficient design is obtained for CSLA. Due to small carry-output delay, the proposed CSLA design is a good candidate for SQRT adder.

Keywords: Adder, BEC, Low power design, CSLA

I. INTRODUCTION

High-speed data path logic systems are one of the most substantial areas of research in VLSI system design. High performance, low power and area-efficient systems are increasingly used in portable devices. A complex digital signal processing (DSP) system involves several adders. An adder is the main component of an arithmetic unit. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing to execute various algorithms like FFT, IIR and FIR. On the basis of requirements such as area, delay and power consumption some of the complex adders are Ripple Carry Adder, Carry look-Ahead Adder and Carry Select Adder. Ripple Carry Adder (RCA) shows the compact design but their computation time is longer. Time critical applications make use of Carry Look-Ahead Adder (CLA) to derive fast results but it leads to increase in area. But the carry select adder provides a compromise between the small areas but longer delay of RCA and large area with small delay of Carry Look Ahead adder. A ripple carry adder uses a simple design, but carry propagation delay (CPD) is the main concern in this adder. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

II. RELATED WORKS

[1] Carry Select Adder Using Common Boolean Logic

In Proposed Sqrt CSLA using Common Boolean Logic to remove the duplicate adder cells in the conventional CSLA, an area efficient SQRT CSLA is proposed by sharing Common Boolean Logic (CBL) term. While analyzing single bit full adder, results show that the output of summation signal as carry-in signal is logic "0" is inverse signal of itself as carry-in signal is logic "1". To share the Common Boolean Logic term, we only need to implement a XOR gate and one INV gate to generate the summation pair. And to generate the carry pair, we need to implement one OR gate and one AND gate. In this way, the summation and carry circuits can be kept parallel. This method replaces the Binary to Excess-1 converter add one circuit by common Boolean logic. As compared with modified SQRT CSLA, the proposed structure is little bit faster. In the proposed SQRT CSLA, the transistor count is trade-off with the speed in order to achieve lower power delay product. This work has been designed for 8-bit, 16-bit and 64-bit word size and results are evaluated for parameters like area, delay and power. It cannot be used for higher number of bits.

[2] Carry select adder using BEC and RCA

The Carry select adder (CSLA) is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input, then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA to achieve high speed and low power.

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In this paper, qualitative evaluations of the CSLA adder with and without BEC architectures are given. Among the huge member of the adders they wrote VERILOG (Hardware Description Language) code for Carry skip and carry select adders to emphasize the common performance properties belong to their classes. With respect to delay time and power consumption this paper concludes that the implementation of CSLA with BEC is efficient. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure consumption.

[3] An area-efficient carry select adder design by sharing the common Boolean logic term

An area-efficient carry select adder is proposed by sharing the common Boolean logic term. After logic simplification and sharing partial circuit, one XOR gate and one inverter gate in each summation operation as well as one AND gate and one inverter gate in each carry-out operation is needed. Through the multiplexer, correct output result is selected according to the logic state of carry-in signal. In this way, the transistor count in a 32-bit carry select adder can be greatly reduced. Moreover, the power consumption can be reduced as well as power delay product reduced.

[4] Lower Power High Performance Carry Select Adder

This work uses a sophisticated and efficient gate-level modification to significantly reduce the delay and power of the carry select adder and observing the structure of the CSA, it is clear that there is scope for reducing the delay and power consumption in the CSA. Based on this modification 8-, 16-, 32-, and 64-bit CSA architecture have been developed and compared with the regular CSA architecture. The proposed design has reduced delay as compared with the regular CSA with only a slight increase in area. This work evaluates the performance of the proposed designs in terms of delay, area, power, and their products by hand with using tools like synopsis (VCS), Xilinx ISE. The results analysis shows that the proposed CSA structure is better than the regular CSA according to delay.

[5] An Efficient 64-Bit Carry Select Adder With Less Delay And Reduced Area Application

In this paper an efficient approach is used to reduce the area and delay of SQRT CSLA architecture. The reduction in the number of gates is obtained by simply replacing the RCA with BEC in the structure. The compared results shows that the modified SQRT CSLA has a slightly larger area for lower order bits which further reduces for higher order bits. The delay is reduced to a great extent with the modified SQRT CSLA. This results shows that using modified method the area and delay will decrease thus leads to good alternative for adder implementation for many processors. This approach is suitable only for lower order bits, it is not possible for higher order bits like 128,256 and more.

III. METHODOLOGY

1. Conventional Carry Select Adder

CSLA uses RCA to generate sum and carry values using initial carry as 0 and 1 respectively, before the actually carry arrives in. Upper RCA is given with carry initial value as logic "0" while lower RCA is given with carry initial value as logic "1". Multiplexer selects the result of carry "0" path if the previous carry is logic '0' or the result of carry "1" path if the previous carry is logic '1' i.e., actual carry is used to select the sum and carry using a multiplexer. Each RCA pair in CSLA can compute in parallel the value of sum before the previous stage carry comes. Thus, the critical path of an N bit adder is reduced. Delay in CSLA is much lesser than RCA because the critical path in case of conventional adder is N-bit carry propagation path and one sum generating stage while in case of CSLA, the critical path is (N/L)-bit carry propagation path and L stage multiplexer with one sum generating stage in the N- bit CSLA, where L is number of stages in CSLA. Since L is much less than N and multiplexer delay is less than the delay in full adder, hence the delay in the CSLA is much less than that in the RCA but there exists copy of hardware in each stage which leads to an increase in the amount of power consumption and cost.

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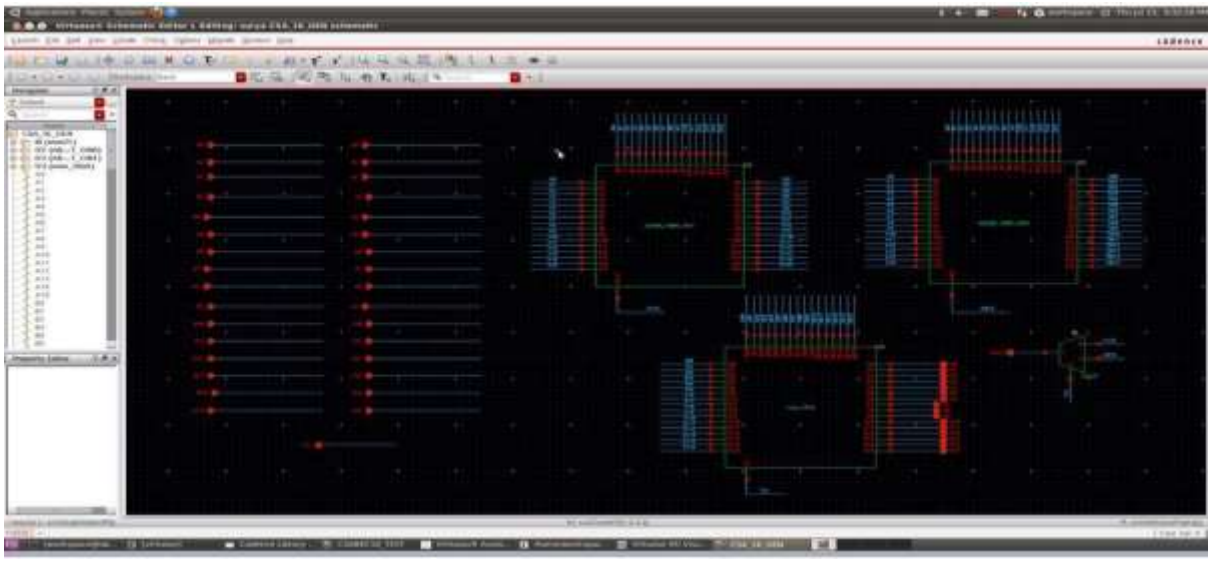

Figure 3.1. Schematic of Conventional Carry Select Adder

2. Binary To Excess-1 Convertor Carry Select Adder

The BEC- CLSA uses RCA to generate sum and carry values using initial carry as 0. The BEC unit then receives and c 0 out from the above RCA and generates (n + 1)-bit excess-1 code. A BEC is a combination of XOR gates in conjugation with AND gates such that each and gate acts as an internal carry generator circuit that generates the carry of the two consecutive sum bits. The first sum bit S0 of the first stage RCA is passed through an inverter and inverted bit is taken as the first sum bit of add one operation. The first sum bit of first stage of RCA is ANDed with the second sum bit of first stage RCA, so as to generate the first internal carry bit. This carry bit generated is summed with third sum bit of the first stage RCA. The same process of generation of the carry from first stage sum bits and summation of consecutive internally generated carry bits with previous sum bits gives the overall add one operation using BEC logic. Thus, we obtain the final sum bits for both the possibilities of carry being 0 by first stage RCA and carry being 1 by BEC logic block. These two sequences are sent to a final stage MUX array which selects any of the two sequences based on the previous stage carry being either 0 or 1. Using this method, we have three design advantages

(i) Calculation of s 0 1 is avoided in the SCG unit

(ii) The n-bit select unit is required instead of (n + 1)- bit

(iii) Less output-carry delay.

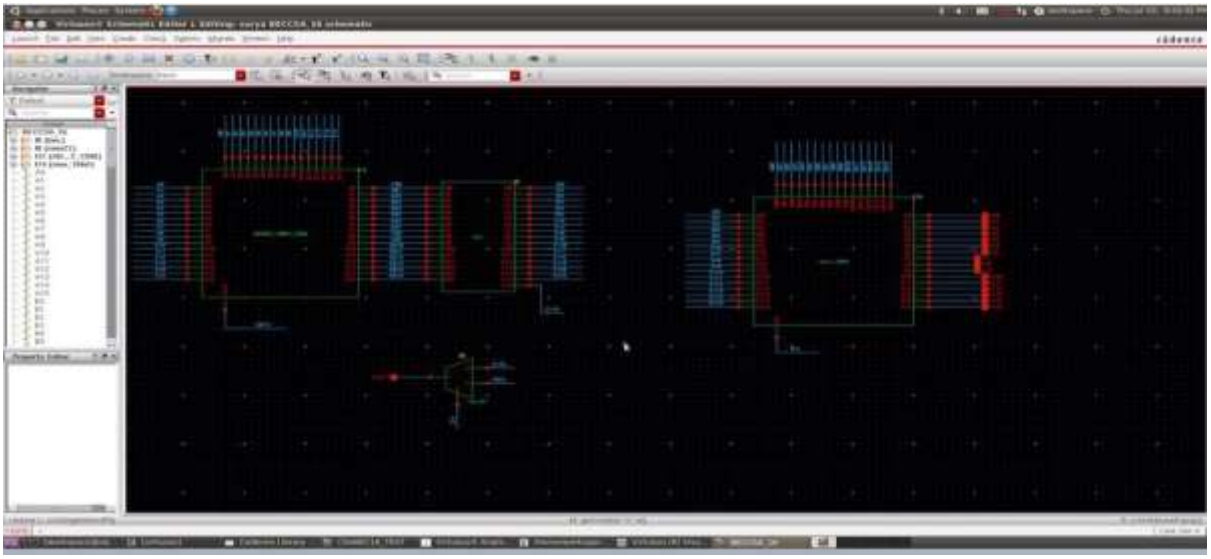

Figure 3.2. Schematic of Binary to Excess-1 Convertor

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3. Proposed Carry Select Adder

It consists of one HSG unit, one FSG unit, one CG unit and one CS unit. The CG unit is comprised of two carry-generators (CG0 and CG1) corresponding to input-carry '0' and '1'. The HSG receives two n bit operands (A and B), and generate half-sum word s0 and half-carry word c0 of width n-bit each. Both CG0 and CG1 receive s0 and c0 from the HSG unit and generates two n-bit full-carry words c01 and c11 corresponding to input carry '0' and '1', respectively. The logic circuits of CG0 and CG1 are optimized to take advantage of the fixed input carry bits. The CS unit selects one final-carry word from the two carry words available at its input-line using control signal FSG unit consists of XOR gates. The input s_0 and c_n is XORed and output sum s_0 is obtained.

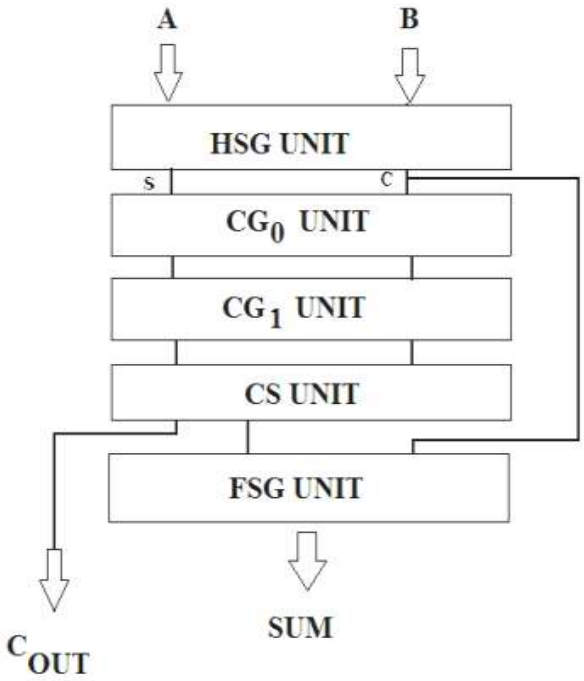

Figure 3.3. Block Diagram of Proposed Carry Select Adder

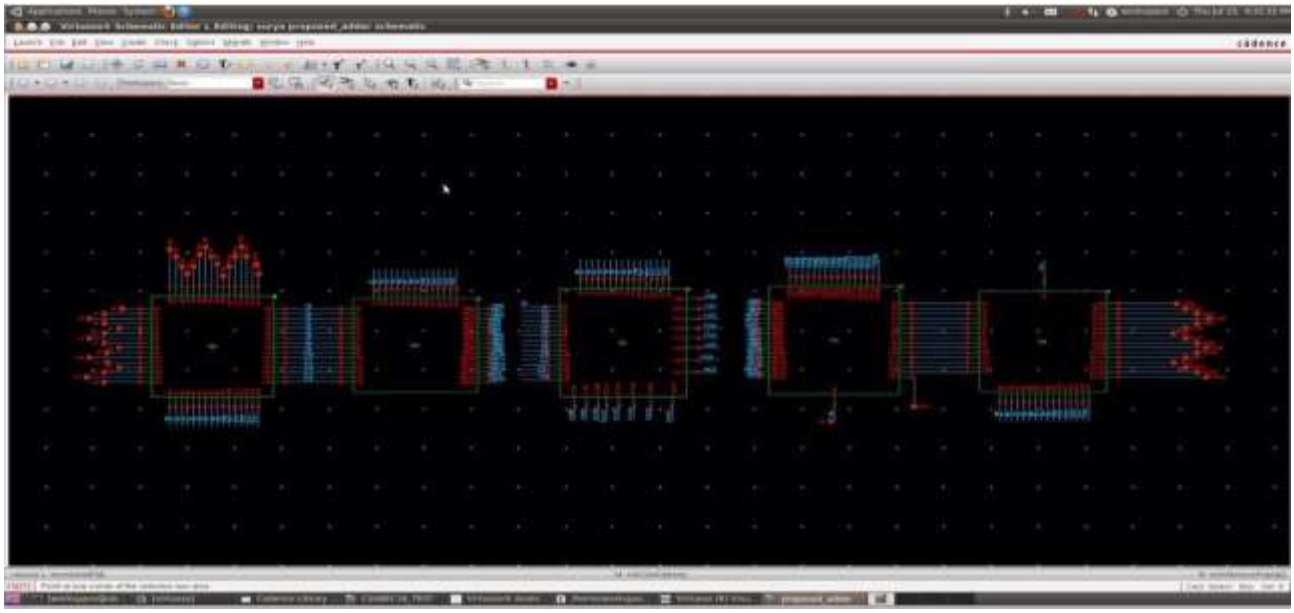

Figure 3.4. Schematic of Proposed Carry Select Adder

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4. Square Root Carry Select Adder

Square Root Carry Select Adder (SQRT CSLA) is one of the fastest adders which is used in this data-processing processor to perform fast arithmetic functions. The Carry Select Adder based Common Boolean Logic (CSLA-CBL) involves significantly less logic resource than the conventional Carry Select Adder (CSLA) but it has longer Carry Propagation Delay which is almost equals to that of Ripple Carry Adder (RCA). To overcome this problem, here, an area-efficient Square Root Carry Select Adder (SQRT CSLA) by sharing Common Boolean logic term (CBL) is designed, the modified architecture has been developed using Binary to Excess-1 converter (BEC). The proposed CSLA design involves significantly less area and delay than the previously proposed CSLA-BEC. Theoretical estimate shows that the proposed SQRT-CSLA involves nearly less delay and less area than the conventional CSLA proposed CSLA-BEC.

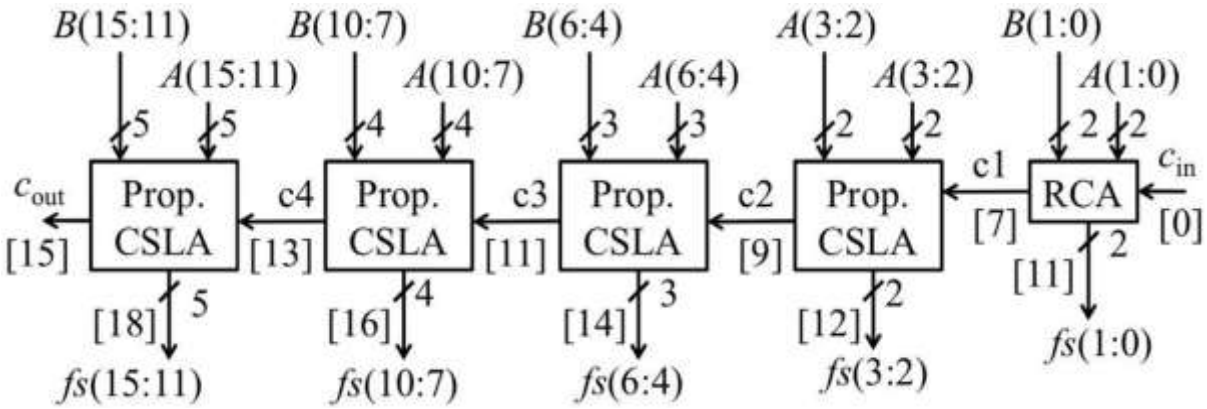

Figure 3.5. Proposed 16-bit Square Root Carry Select Adder (SQRT-CSLA)

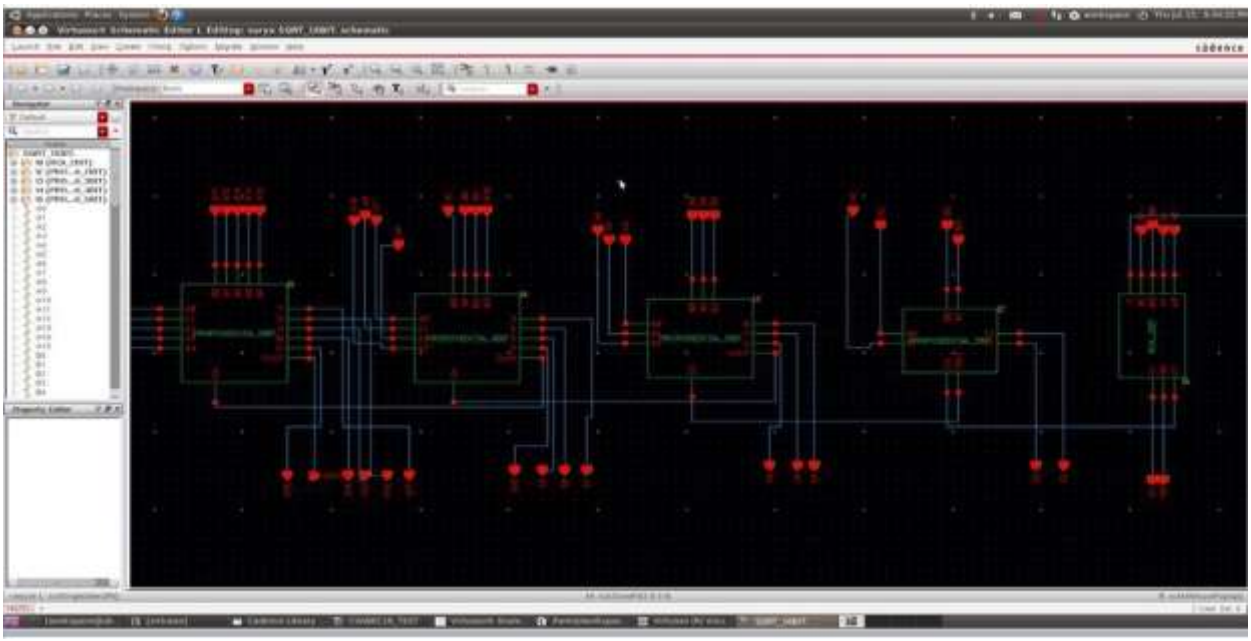

Figure 3.6. Schematic of SQRT CSLA

IV. RESULTS

Table 4.1 Proposed Adder Gate Count

Unit	XOR-Gate	AND-Gate	OR-Gate
HSG	16	16	-
CG	32	32	-

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CSU	-	16	16
FSG	16	-	-
Total	64	64	16

Gate count of the Proposed CSLA Adder is given in the above table 4.1. The HSG block contains 16 XOR gates and 16 AND gates total of 32 gates. CG block is divided into CG0 and CG1 Block, each CG Block contains 32 XOR gates and 32 AND gates, so total CG block contains 64 gates. The CSU block comprises of 16 XOR gates and 16 OR gates and the final block i.e., FSG block that contains 16 XOR gates.
So, by combining all the blocks we have total 144 gates in the Proposed CSLA. But in the conventional CSLA block we use 288 transmission gates to build the circuit. When compared with the BEC-CSLA the BEC has 220 gates so our proposed adder uses less gates when compared with other. SQRT based CSLA has total of 128 gates which is much less than our proposed adder.

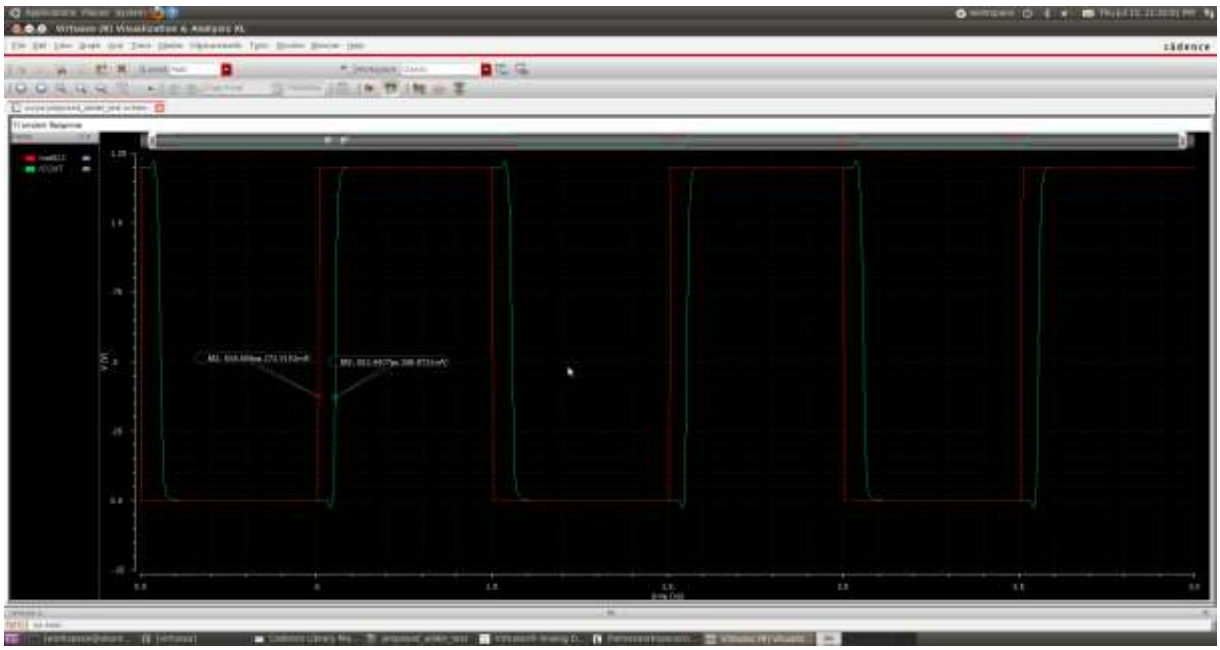

Figure 4.1 Delay of Proposed Adder

In the above figure we can observe the delay of Proposed Adder. Here we get the delay by subtracting the value of M1 and M2 points, so we get the delay of 46.16ps which is less than the Conventional CSLA and BEC based CSLA. In conventional CSLA we get the delay of 65.15ps and in BEC based CSLA we get delay of 56.13ps. So when compared to all other methods our Proposed adder has less delay.
The Figure 3.2 shows the Area values of AND, XOR, INVERTER and MUX. In Layout suite editing we get to know the length and breadth of each. Then value of each is calculated by multiplying with number gates used in units such as CG, CS, HSG and FSG. With this calculation we get HSG area as 342.644 um^2, and value of CG as 684.768um^2, and FSG as 220.224um^2. We get the total area of the Proposed Adder by adding all the block areas. Total area obtained is 1385.31um^2. Area of the conventional CSLA is 2554.68um^2 and the area of BEC based CSLA is 1635.33um^2. So when compared with the other methods our proposed adder consumes less delay. SQRT based CSLA which is the application of our adder consumes much more less delay which is 1289.07um^2.

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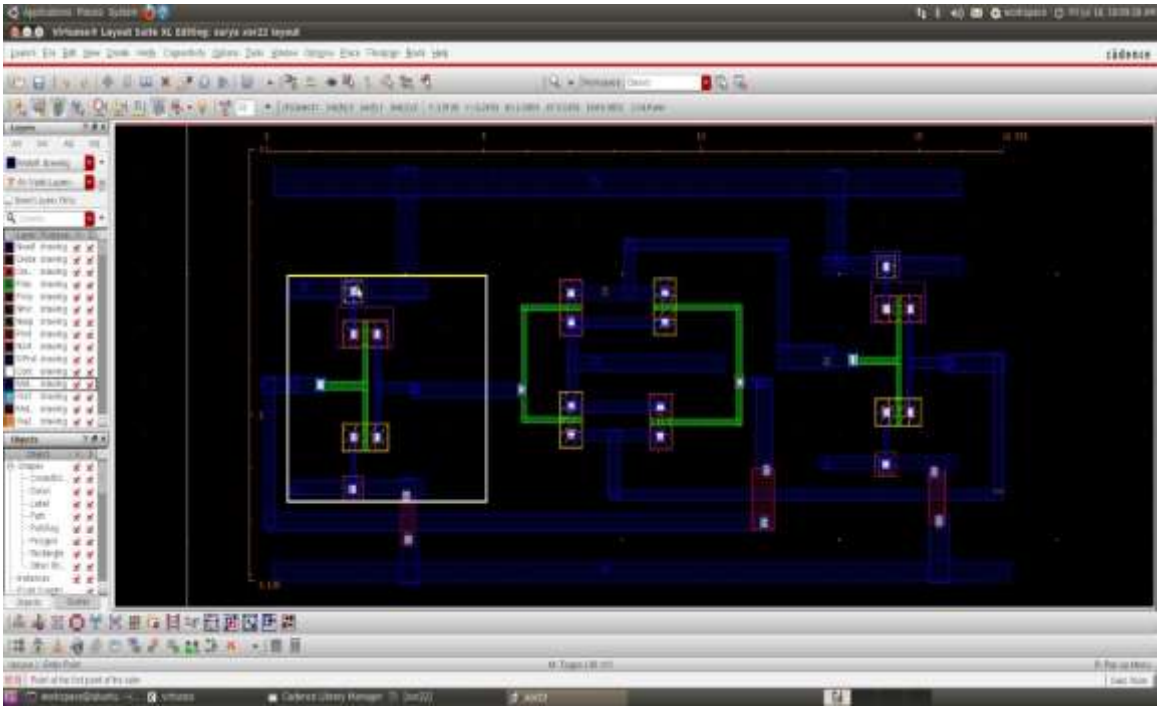

Fig 4.2 Area of XOR gate

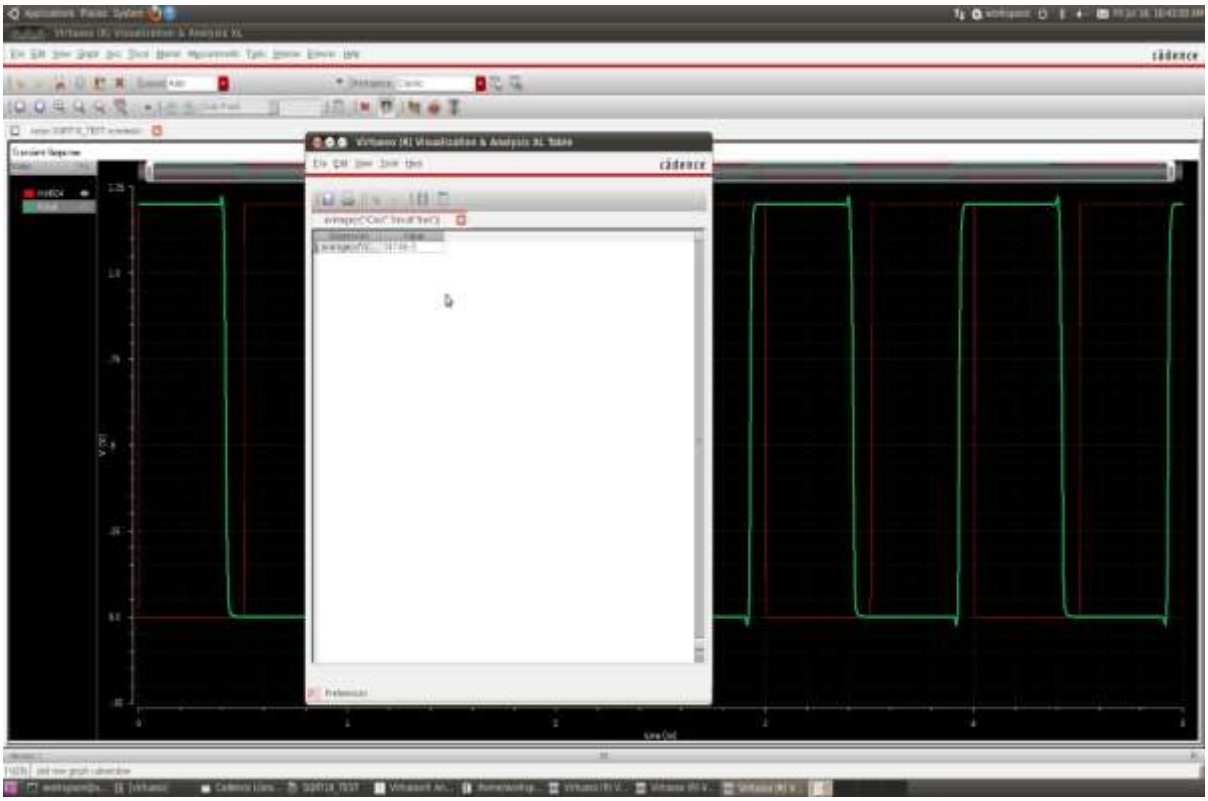

Figure 4.3 Power of Proposed Adder

The above figures show the power values of Carry Select Adder discussed. For Conventional CSLA the power value is 600mW. Similarly, for BEC CSLA we get 592mW. For Proposed CSLA we get 587mW. We are not using transmission gates in the proposed adder so there is no much efficiency in the power reduction.

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Table 4.2 comparison of CSLA

CSLA	No. of Gates	Area	Delay	Power
Conventional CSLA	288	2554.68um^2	65.15ps	600mW
BEC CSLA	220	1635.33um^2	56.13ps	592mW
Proposed CSLA	144	1385.31um^2	46.16ps	587mW
SQRT CSLA	128	1289.09um^2	43.21ps	585mW

V. CONCLUSION AND FURTHER WORKS

As an analysis is made on the logic operations involved in conventional CSLA and CSLA based on binary to excess-1 converter (CSLA-BEC) to study the data dependency and to find redundant logic operations. Now comparing the above CSLAs with respect to the proposed carry select adder which is optimized in delay power among the adders, power consumption and also with reduced in number of transistors. As the conventional CSLA consists a total of 288 transmission gates, CSLA-BEC consists upto 220 transmission gates and the proposed CSLA consists a total of 144 transmissions gates. Hence it is evident that approximately 50% and 35% reduction in gates, are seen in conventional CSLA and CLSA-BEC respectively. As a result of reduction in the number of gates used, the delay of the proposed CSLA is also reduced in comparison with the other 2 CSLAs. The proposed CSLA records delay which is 28% and 17.5% lesser than the conventional CSLA and CLSA-BEC respectively. Even the power consumption is lesser in the proposed CSLA than the other 2 CSLA. Comparing the area utilized by the 3 different CSLA, we find that the proposed CSLA utilizes less area than the other two CSLA. We see the reduction in the area used by the proposed CSLA, that is 46% less than the conventional CSLA and 15% less than that of the CLSA-BEC. Further, the application of the proposed CSLA, that is SQRT CSLA which is designed based on the proposed CSLA gives further reduction in the area, delay and the power is comparison to the proposed CSLA. A nominal reduction of 11% is obtained in the number of gates used. Area and delay both are further reduced by 7%, and a very small reduction is seen in power consumption.
The overall objectives of this project is achieved, as the desired output is obtained in all the fields of interest, and thus the proposed CSLA is more efficient than the other CSLAs,
We can use this adder in various applications and speed up the devices with different specifications as required.

This work has been designed for 16-bit word size and results are evaluated for parameters like area, delay and power. This work can be further extended for higher number of bits. New architectures can be designed in order to reduce the power, area and delay of the circuits. Steps may be taken to optimize the other parameters like frequency, number of gate clocks, length, etc.

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