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Analysis of CMOS Based Folded Cascode Amplifiers

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Abstract: In this paper, analysis of low voltage folded cascode Op Amp based on different voltages has done at 45nm. DC voltage gain, average power, Unity gain bandwidth and output resistance have been compared at different voltages. Low voltage folded cascode Op Amp results in high performance.

Keywords: DC Voltage Gain, Average Power, Unity Gain Bandwidth and Output Resistance

I. INTRODUCTION

Supply voltage reduction guarantee the reliability of devices as the lower electrical fields inside layers of a MOSFET produces less risk to the thinner oxides, which results from device scaling. However, the reduction in supply voltage leads to degraded circuit performance in terms of available bandwidth and voltage swing. Scaling down the threshold voltage of the MOSFETs reduces the performance (degraded bandwidth, low voltage swing etc.) to some extent but there is increase in the static power dissipation. The performance analysis of conventional Op Amps techniques at large channel length is going to out of reach in near future. The appropriate topology is suggested which has a perfect balance between complexity and performance. Scaling of Complementary Metal-Oxide Semiconductor (CMOS) technology to the nano ranges has many limitations and leads to increase the leakage currents, power dissipation, and short-channel effects. The Figure 1 shows the schematic of a folded-folded cascode op-amp using a class AB output buffer. In the frequency response of the op-amp, the load of the op-amp is a 1 pF capacitor. Folded cascode Operational Amplifier is designed at different voltages. The widths of MOSFETs are chosen to be identical for a reasonable comparison [1-7].

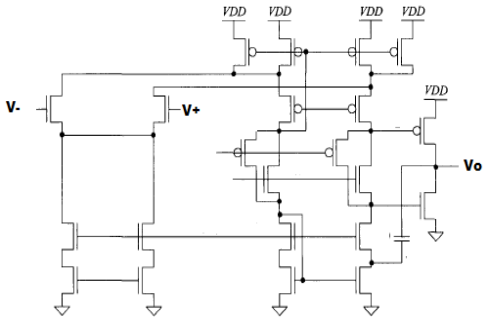

Fig 1. Folded Cascode Op Amp Design

II. FOLDED CASCODE OP AMP DESIGN

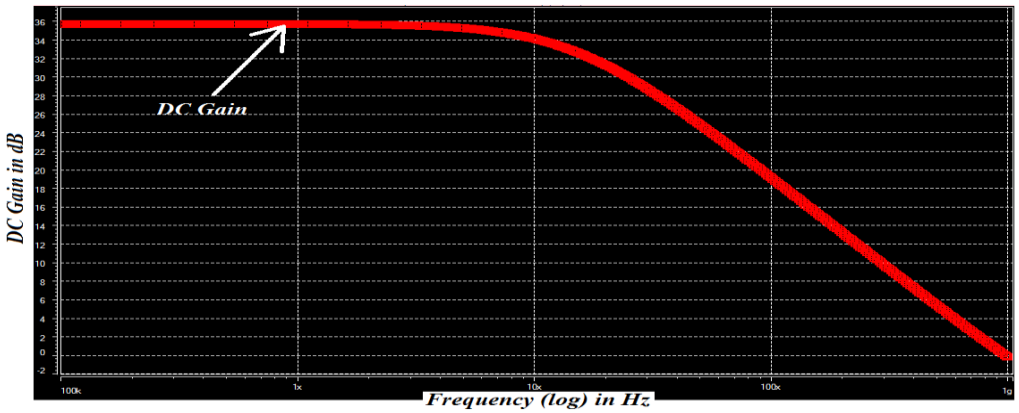

Fig 2: Frequency response of CMOS based folded cascode op amp design at 1.4V

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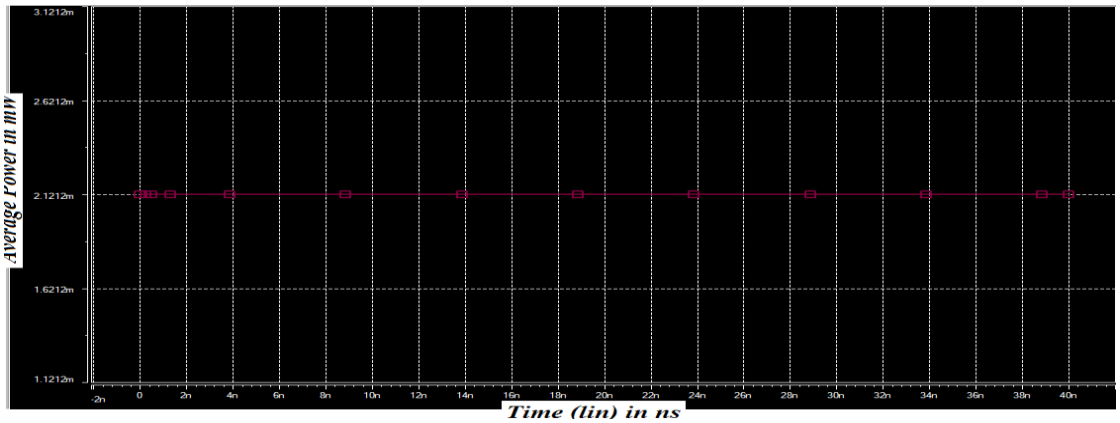

Fig 3: Average Power of CMOS based folded cascode op amp design at 1.4V

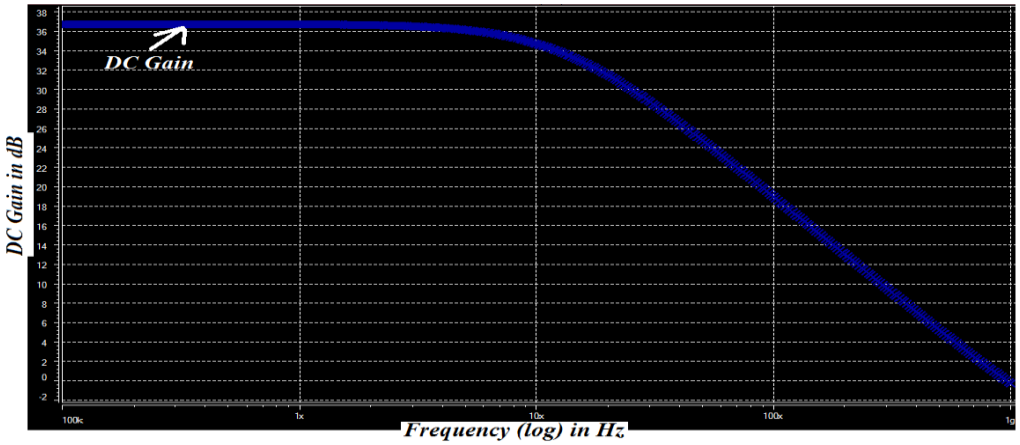

Fig 4: Frequency response of CMOS based folded cascode op amp design at 1.2V

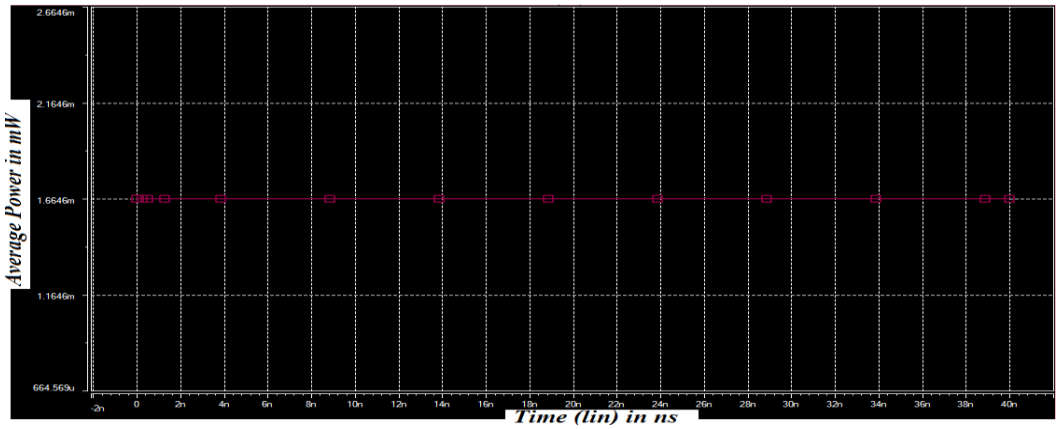

Fig 5: Average Power of CMOS based folded cascode op amp design at 1.2V

Table: Comparative analysis of Folded Cascode Op Amp Design with CL = 1 pf , at different V_{DD}

S. NO.	PARAMETERS	CMOS BASED FOLDED CASCODE AMPLIFIER AT 1V	CMOS BASED FOLDED CASCODE AMPLIFIER AT 1.2V	CMOS BASED FOLDED CASCODE AMPLIFIER AT 1.4 V
1	DC GAIN	37.6 dB	36.7 dB	35.7 dB
2	Unity Gain Freq	951 MHz	963 MHz	978 MHz
3	Output Resistance	23.1 Ohms	23.4 Ohms	24 Ohms
4	Average Power	1.24mW	1.66mW	2.12 mW
5	Phase Margin	79.20	80.50	810

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III. CONCLUSION

In this research paper, analysis of low voltage folded cascode Op Amp based on different voltages has done at 45nm. DC voltage gain, average power, Unity gain bandwidth and output resistance have been studied. Low voltage folded cascode Op Amp results in high performance. The proposed low voltage Cascode Op Amp is better for applications in VLSI design for low voltage applications.

REFERENCES

[1]. Gulati, K., & Lee, H.-S. (1998). A high-swing CMOS telescopic operational amplifier. IEEE J Solid-State Circuits, 33(12), 2010–2019.
[2]. Nakamura, K., & Richard Carley, L. (1992). An enhanced fully differential folded-cascode Op-Amp. IEEE Journal of Solid-State Circuits, 27(4), 563–568.
[3]. Musah, T., Gregoire, B. R., Naviasky, E., & Moon, U. (2007). Parallel correlated double sampling technique for pipelined analogue-to-digital converters. Electron Letter, 43(23), 1260–1261.
[4]. Gregoire, B. R., & Moon, U. (2008). An over-60 dB true rail-torail performance using correlated level shifting and an opamp with only 30 dB loop gain. IEEE Journal of Soild-State Circuits, 43(12), 2a620–2630.
[5]. Laber, C. A., & Gray, P. R. (1988). A positive-feedback transconductance amplifier with applications to high-frequency, highQ CMOS switched-capacitor filters. IEEE Journal of Solid-State Circuits, 23(6), 1370–1378.
[6]. Ramirez-Angulo, J., Calvo, B., Carvajal, R., Lopez-Martin, A. (2010) Low-voltage gm-enhanced CMOS differential pairs using positive feedback (pp. 773–776). Paris, France: IEEE ISCAS
[7]. Razavi, B. (2001). Design of analog CMOS integrated circuits. McGraw-Hill. 8. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. (2001). Analysis and design of analog integrated circuits. New York: Wiley