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Simulation of Modular Multilevel Step-Down DC-DC Converter for Renewable Energy Applications

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Abstract: This paper proposes to achieve an high step-down ratio by using MMC DC-DC converter topology and maintaining high conversion efficiency with high power rating. For High step down ratio dc-dc power conversion power electronics transformers are can be used. This arrangement requires a large number of high isolation voltage transformers and complicated balancing control. To overcome this drawback the solution is inherent voltage balancing, this paper introduces a new MMC topology for dc-dc conversion. Depending on the number of sub modules the MMC achieves high-voltage step-down ratio. With no necessary requirement of high-voltage isolation transformers the converter exhibits simplicity and scalability by using Digital switching, the converter operating frequency is high compared to the switching frequency. The operation principle and theoretical analysis are presented in this paper.

Keywords: Modular multilevel converter (MMCs), phase-shift control, step-down ratio, resonant converter, DC-DC conversion.

1. INTRODUCTION

In case of medium-voltage and high-voltage applications Modular multilevel converters (MMCs) are can be used, for ac-ac[9],[10],ac-dc [4],[6]-[8],dc-dc[11]-[13],dc-ac,[1]-5]conversion.By changing the number of modular cells, these converters provide more than two levels. While keeping the converters operating cells with a fault can also be bypassed. The main features of MMCs are High reliability and modularity. To maintain the voltage levels all these MMCs require a complicated balancing control. Even though a requirement is placed on the tolerance of the cell capacitors, measuring capacitor voltages for balancing control is indispensable. The operating frequency of the MMCs is not higher than the switching frequency. To reduce the size of the passive components High switching frequencies are used. Low-power applications other new multilevel modular switched capacitor dc-dc converters designed [14]-[16]. This type converter exhibit good efficiency and modularity, but these type converters not suitable for high-voltage applications. Conventional diode clamped, flying capacitor, or other types of converters are also not suitable for the high voltage applications, as the circuit configuration becomes quite complicated with increased number of levels[17],[18].These converters have poor modularity and reliability .For high power applications other type converter is Power electronic transformers (PETs) [11], [12], [19], [20]. These type converters require a large number of transformers with high-voltage isolation. The balancing control between the modules is necessary. For high-voltage and high-power applications PETs are can be used with high efficiency, but the converter size will be increased dramatically with a high-voltage step down ratio. In this paper for high-voltage step-down unidirectional dc-dc conversion [13] a new form of MMCs are introduced.

By using large number of sub modules High step-down voltage conversion ratios can be achieved. The proposed converter has inherent-balancing of each capacitor voltage. For Higher operating frequency, phase-shifted pulse width-modulation (PWM) technique is used. This is equal to the product of the number of sub modules and the switching frequency. The converter operates with two resonant frequencies where zero voltage-switching (ZVS) and zero-current-switching(ZCS) become possible. The pro-posed converters are more suitable for low-power dc-dc applications. Multilevel inverter provides a suitable solution for medium and high power systems to synthesis output voltage which allows a reduction of harmonic content in voltage and current waveforms. The main features of these converters are modularity, simplicity, and flexibility.
Modular multi level converter fully modular converters benefit from several advantages such as:

1) The ability to control the voltage and current stresses applied to their components through incur-poration of identical modules in series or parallel;

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2) enhanced reliability through installation of redundant modules;
3) reduced design, manufacturing, installation, and maintenance cost. The detailed configuration and operation principle are presented.

2. SYSTEM STRUCTURE, MODELING AND CONTROL.

2.1 SWITCHING STRATEGIES

In conventional approach, PWM techniques are used by the comparison of reference and carrier signals to provide the required gating signals for the converter switches. The number of output voltage levels obtained from this approach is given in the following equation.

$$m = 2Ns + 1$$

Where m denotes the output voltage levels and N_s is the individuals' converter stages. The number of switches (*l)* required to achieve m levels is given in the following equation.

$$l = 2(m - 1)$$

For the implementation of 15-level CMLI, the number of switches required is 28 with seven individual inverter stages. In addition to the 28 switches, 182 clamping diodes in case of NPC or diode clamped multilevel inverter and 91 balancing capacitors in case of FC type multilevel inverter along with 14 DC bus capacitors are needed to achieve 15-level output. The proposed paper deals with the following topologies for the reduction of switches. Increasing the number of levels will subsequently reduce the harmonic distortion which in turn improves the power quality. By using large number of sub modules High step-down voltage conversion ratios can be achieved. The proposed converter has inherent-balancing of each capacitor voltage. For Higher operating frequency, phase-shifted pulse width-modulation (PWM) technique is used. This is equal to the product of the number of sub modules and the switching frequency.

2.2 Phase-Shifted PWM for High Step-Down Ratio.

Phase-shifted PWM is then applied with a high duty-ratio such that an excitation is applied to the resonant components. The effective frequency of this excitation is much higher than the frequency of switching of an individual cell [21], [22].This is arranged so that only one cell at a time is in "zero state," and thus, the step-down ratio of the circuit becomes dependent on the number of cells *N*. To demonstrate the general operation. The dc input Voltage is V_{dc}.
The capacitor voltage and output voltage of j_{th}(j = 1, 2, . . . , 5) cell are represented by $VC_j$and V_j, respectively. The input current $i_s$is composed of the dc component and ac component. The dc current component returns to the converter input mainly through the parallel inductor *Ls*, where an ac current component mainly flows to the rectifier. The sum of the parallel inductor current $i_p$and the rectifier input current$i_t$is equal to i_s.
The switching frequencies and duty-ratios of cells are equal, but the PWM signals from Cell 1 to Cell 5 are shifted by 0◦, 72◦, 144◦,216◦, and 288◦, respectively. To analyze the circuit operation, the following assumptions are made:
1) The switches are lossless and the cells are identical with the same parameters.
2) The cutoff frequency of the input filter is much lower than the series current frequency in the converter. The input ac current and dc current flow through the parallel branch and the series branch of the input filter, respectively.
3) The dc voltages of the cell capacitors are balanced at a steady state.
4) The rectifier diodes are synchronously switched ON with the rectifier input voltage.

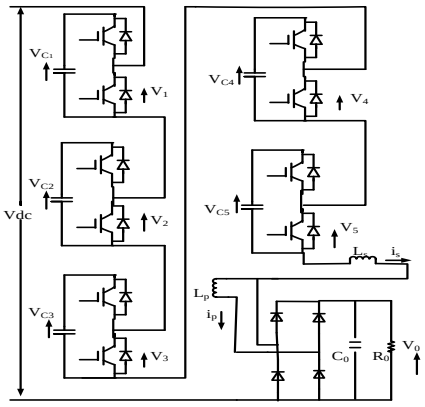

Fig.1. Five-cell step-down series-parallel resonant converter.

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3. RESONANT OPERATION AND INHERENT-BALANCING

This section presents the analysis of the equivalent operation of the first configuration (see Fig.1).The operation principle of other configurations can be analyzed by using the similar method. To demonstrate the operation principle in a simple way, the starting point is selected at the time when the capacitor of Cell 1 mode with dead band, there are four operation modes in each operating cycle,

3.1 Modes of operation.

Mode:1

The circuit consists of four modes of operation in each operating cycle, we assume the parallel current **ip** is above zero. when the lower cell1 is turned OFF, and the circuit enters the dead time mode. In this mode, no current flows through cell and all the current circulates between the parallel inductor and rectifier. After a short time, the upper switch in cell 1is turned ON and the circuit enters mode 2.The output voltage is positive $V_{dc.}$ All the cell capacitors are in series with the inductor L_s. The input voltage of the rectifier is negative. The input current i_t is negative. This mode lasts until the upper switch of cell 2 is turned OFF. and the circuit enters the dead time mode.

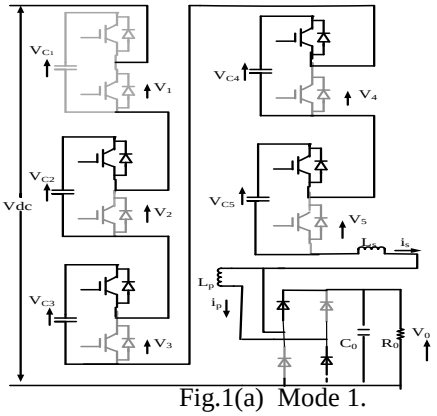

Fig.1(a) Mode 1.

Mode:2

In this mode of operation all the cell capacitors are in series with the inductor L_s. The input voltage of the rectifier is negative, and the input current $i_t$is negative. In this mode five capacitors are in series, the input voltage of the rectifier is negative(V_t<0). The resonant current flowing through relevant diodes, $V_t$is clamped by the output voltage as V_t= -V_0. If the output current does not fall to Zero before the half T_e, the converter is operating in the continuous conduction mode(CCM). Otherwise it may operate in the discontinuous conduction mode. When the I_o falls to zero the output is disconnected from the parallel inductor L_p and V_t is dependent on the current $I_p$until the next switching action occurs. The output current $i_o$is rectified from i_t. where five capacitors are in series, the input voltage of the rectifier is negative (vt<0). With the resonant current flowing through relevant diodes, $vt$is clamped by the output voltage as $vt = -vo$.

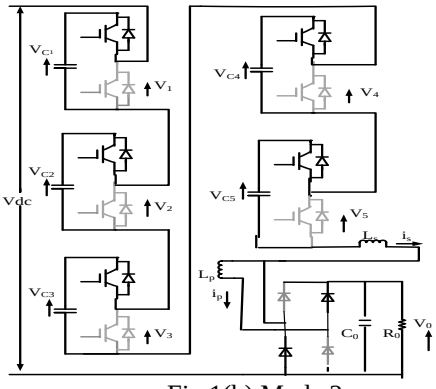

Fig.1(b) Mode 2

The output current does not fall to zero before the half *Te*, the converter is operating in the continuous conduction mode (CCM).Otherwise, it may operate in the discontinuous conduction mode (DCM). When *io*falls to zero, the output is disconnected from the parallel inductor *Lp* and *vt*is dependent on the current *ip*until the next switching action occurs.

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On the other hand, in the last mode, one capacitor is out and four capacitors join the series resonance. The input voltage of the rectifier is clamped as *vt= vo*as long as the converter operates in the CCM. If *io*falls to zero before this half operating cycle, the operation mode becomes the DCM and *is = ip*until the end of this operating cycle.

Mode:3

This mode is the dead time mode of Cell 2. As there is no series current, all the current on the parallel inductor flows to the diode rectifier. Shortly after that, the lower switch of Cell 2 is turned ON and the circuit becomes another resonant circuit only with capacitors of Cells 1, 3, 4, and 5 in series with *Ls.* As *vt* becomes positive in this mode, the series current starts to rise with its resonant waveform. This mode is dead time mode of cell 2 .As there is no series current ,all the current on the parallel inductor flows to the diode rectifier after the small time period the lower switch of cell 2 is turned ON.The circuit becomes another resonant circuit only with capacitors of cell1,3,4,5 in series with L_s and V_t becomes positive in this mode ,the series current starts to rise with its resonant wave form.

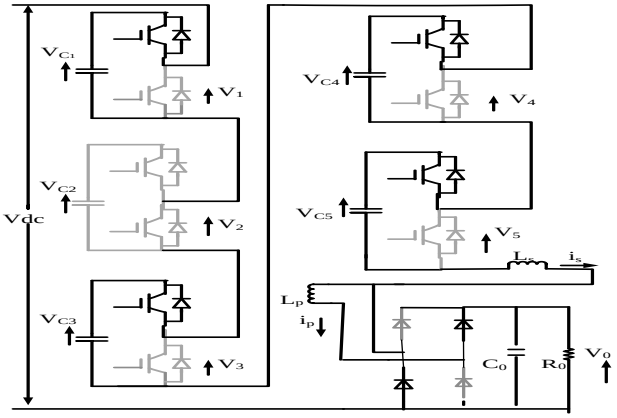

Fig.1(c) Mode 3

Mode :4

In this mode of operation one capacitor is out and four capacitors join the series resonance .The input voltage of the rectifier is clamped as $V_t=V_0$ as long as the converter operates in continuous conduction mode. If I_0 falls to zero before this half cycle operating cycle, the operation mode becomes the discontinuous conduction mode and $I_s=I_p$ until the end of this operating cycle. For each T_e half cycle all five cells are operates with back to back operation there are always five capacitors in the series resonant operation. In the next cycle *Te*, the capacitor of Cell 2 will be in, and later on, the capacitor of Cell 3 will be out. The following capacitors 'in and out sequence should be the capacitors of Cell 3 and Cell 4,the capacitors of Cell 4 and Cell 5, the capacitors of Cell 5 and Cell 1, and finally back to the capacitors of Cell 1 and Cell 2 in the next switching cycle. Hence, there are always five capacitors or four capacitors in the series resonant operation alternatively, with the duration of each mode as half *Te*.The total voltage on the series capacitors is always clamped through the diode bridge by the constant output voltage and the input voltage. When the converter is operating at a steady state, the switching frequency is $f_s$and the duty-ratio of each cell is 90%.Based on the previous assumptions,the key voltage waveforms of the converter are shown in Fig. 2. With the phase-shift control, the output voltage of *j*th cell v*j*is square wave ranging from 0 to the steady-state cell capacitor voltage $\overline{v}C_j$

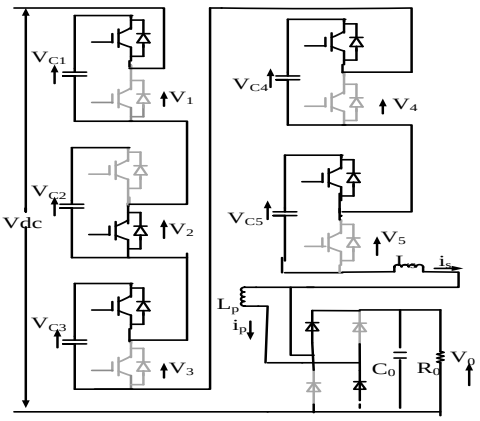

Fig.1(d) Mode 4

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Define output voltage across all the cells as $vs = \sum_{j=1}^{N} vj$ Therefore, $v_s$is ranging from the sum of four cells' capacitor voltages to the sum of five cells' capacitor voltages. As all the cell capacitor voltages are assumed to be equal to $\overline{v}$C, the stack voltage $v_s$is comprised of a square wave ripple with the amplitude of $0.5\,\overline{v}$c and a dc offset of $4.5\overline{v}C$. It can be observed from Fig. 2 that the ripple frequency is five times of the switching frequency. Assume there is no ac voltage drop across the passive components, the rectifier input voltage $v_t$is a square wave with the amplitude of $0.5\overline{v}C$ but in an opposite phase compared to the ripple of v_s. As the dc offset of $v$sis $4.5\overline{v}C$ with N = 5, the cell capacitor voltage can be derived as $\overline{v}C = V$dc/4.5. In a more general case with N cells, the average cell capacitor voltage can be derived as.

$$v\overline{c} = \frac{2Vdc}{2N-1} \qquad (1)$$

with the phase-shift angle of $\frac{360}{N}$and the duty-ratio of$\frac{2N-1}{2N}$.Hence, the peak voltage value of $v_t$is $0.5\overline{v}C$.If the converter output voltage $v_o$is close to the peak input voltage of the rectifier .

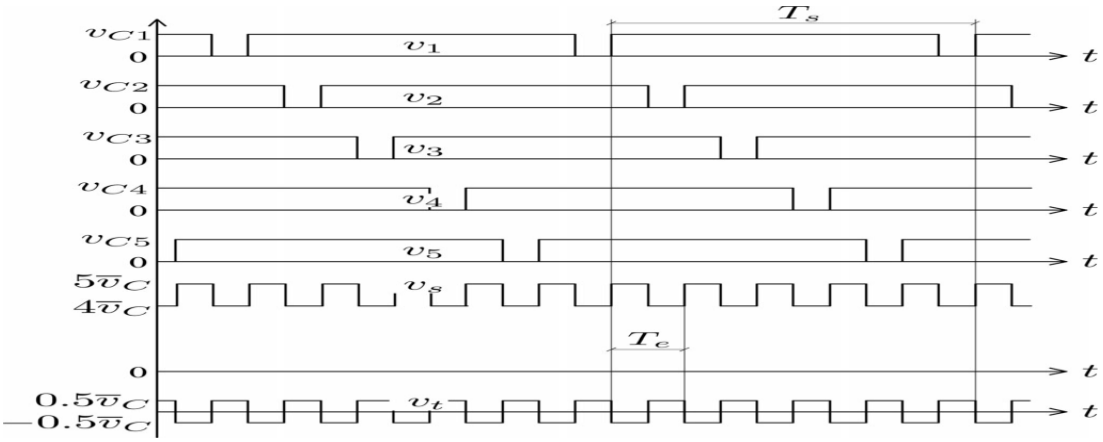

Fig:2.Time-domain key voltage waveforms of the five-cell converter

This converter achieves a step-down ratio of $2N - 1$ which is a function of the number of half-bridge cells. With more cells in the converter, higher step-down voltage ratio can be achieved.

The equivalent operating frequency $f_e$is expressed by

$$fe = Nfs \qquad (2)$$

which is used to choose the passive components for the resonant operation.

Assume that the dc component and root mean square (RMS) value of an ac component of the series current are I_{dc} and I_{ac} ,respectively. If we neglect the losses of the converter, the input power is almost equal to the output power, which can be written as

$$VdcIdc = v\overline{o}Iac \qquad (3)$$

As $V_{dc}/v_o = 2N - 1$, it can be derived from (3) that $I_{ac}=(2N - 1)I_{dc}$. With a rated power P, the RMS of the ac current can be derived as

$$Iac = \frac{(2N-1)P}{Vdc} \qquad (4)$$

This means that when the output power is constant, the current RMS value and switch stress are proportional to the step-down ratio. As the ac current is usually much higher than the dc current, the conduction losses mainly come from the ac current. If we assume that the average voltages across IGBTs and diodes are the same as V_{semi} , the conduction losses caused by the ac current can be written as

$$Pac = IacVsemiN. \qquad (5)$$

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Therefore, comparing *P*ac to the input power, it can be derived that the efficiency η is limited by the conduction losses as

$$\eta < 1 - \frac{N(2N-1)Vsemi}{Vdc} \qquad (6)$$

is involved into the resonant operation and the end point is selected at the time when capacitor of Cell 2 is out of the resonance. The relevant time interval can be found in Fig.2 which is marked by the equivalent operating cycle *Te*. Note that fixed dead time is used for all switches.

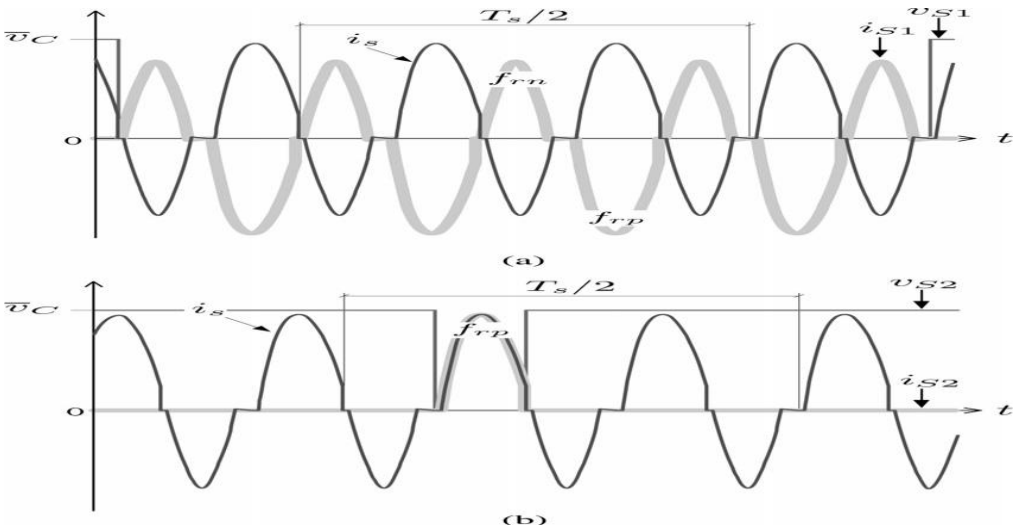

Fig.3. Time-domain waveforms of the voltages and currents of the cell switches. (a) Upper switch. (b) Lower switch.

when a switch is OFF, the current is zero. It can be seen that the converter can achieve ZCS and ZVS for the upper switches, but it cannot achieve soft switching for the lower switches. The turnoff current of the lower switch is high because the operating frequency is higher than the second resonant frequency *frn*. In general, ZCS cannot be achieved for any switch if the operating frequency is higher than the second resonant frequency f_{rn}. On the other hand, if the operating frequency is lower than the first resonant frequency f_{rp}, ZCS and ZVS for upper switches and near ZCS and near ZVS for lower switches are achieved.

3.2 Voltage controller of each cell

The low operating frequency results in high conducting peak current. For most IGBTs, as both the collector–emitter saturation voltage and diode forward voltage increase significantly if the current increases, higher peak current may lead to higher conduction losses. Mean while, the stress on devices is also increased. On the other hand, when the switching frequency increases, switching losses will increase significantly due to the increased times of switching actions. Therefore, a good trade-off according to a practical converter should be made to minimize the total losses. Note that the resonant operation with inherent-balancing of the converter is achieved using a diode rectifier. Thus, the converter topology can only provide unidirectional power flow. The bidirectional operation may be achieved using an active rectifier instead. However, as an active rectifier has three different voltage levels on its ac input side, implementing active voltage clamping for cell capacitor balancing is difficult. This converter topology would require a new control scheme and a different operation method.

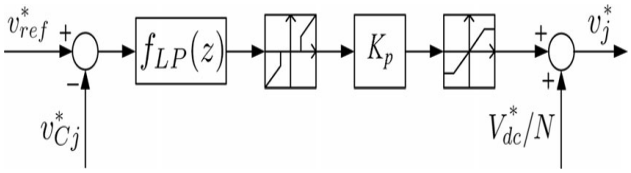

Fig.4. Voltage controller of each cell.

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4. IMPLEMENTATION AND APPLICATIONS

To implement a converter prototype, digital signal processors can be used as the main controller for measuring feedback signals and generating phase-shifted PWM signals. As explained in the previous section, the proposed converter has an inherent-balancing ability. Therefore, the converter can operate under the open-loop condition without using balancing control. However, active balancing control methods can still be used to ensure proper operation under certain circumstances. The performances of the converter with and without balancing control will be compared in the next section. The design of control circuit for a solar fed cascaded multilevel inverter to reduce the number of semiconductor switches is presented in this study. The design includes binary trinary and modified multilevel connection(MMC)-based Topologies suitable for varying input sources from solar photovoltaic's (PV). In binary mode, 2Ns +1 −1 output voltage levels are obtained where Ns is the number of individual inverters. This is achieved by digital logic functions which include counters, flip-flops and logic gates. In trinary mode, 3Ns levels are achieved by corresponding look-up table. MMC intends design in both control and power circuits to provide corresponding output voltage levels by appropriate switching sequences. Hence to obtain a 15-level inverter, the conventional method requires 28 switches and in binary mode 12 switches are Needed. In trinary mode with the same 12 switches, 27 levels can be obtained whereas in MMC only 7 switches are employed to achieve 15 levels. The advantage of these three designs is in the reduction of total harmonic distortion by increasing the levels. Simulations are carried out in MATLAB Simulink and comparisons were made. All the three topologies are experimentally investigated for a 3 kWp solar PV plant and power quality indices were measured.

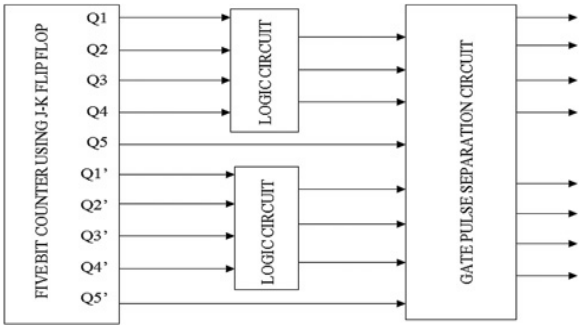

Fig.5. Block diagram of the proposed logic circuit

Fig. 5shows the block diagram for the implementation of the binary mode. The three stage inverter re-quires Ns+ 2 (3 + 2 = 5) bit counters which acts as an up counter. The combinational logic circuit makes the three bits (Q1, Q2 and Q3) to move in forward direction during the first half of the positive half cycle and similarly in reverse direction during second half of the positive half cycle. The same condition is repeated in both half of the negative half cycle. The bits (Q1, Q2 andQ3) are modified by Q4 and Q4′, where Q4′ is used to control the incremental operation in the first half of positive or negative half cycles and Q4 is used for the decrement operation in the latter half of positive or negative half cycles. The pulse separation block comprises of bits Q5'and Q5 to separate the pulses requires for both positive and negative half cycles and also controlling other bits in the circuit. Any number of levels can be achieved with this methodology by only adding the counters as accordance to the number of inverter stages and control logic functions

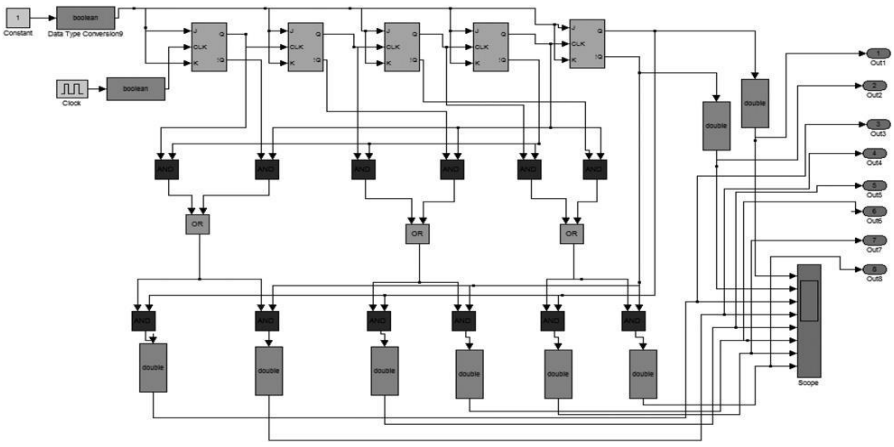

Fig. 6 Digital switching circuit for 15-level CMLI

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Fig. 6 shows the proposed simulation block of the control circuit which consists of counters, combination circuit and pulse separation circuit. The clock signal is given as the input to the five bit asynchronous counter for the movement of bits suitable for positive and negative half cycles as according to the truth table. At logic functions, the pulses are separated and given to the inverter switches. Fig. 7 shows the 15-level output voltage waveform achieved from three stage inverter and its corresponding FFT (fast Fourier transform) analysis.

A. Balancing control

Fig.4 shows the balancing controller of the proposed converter. In order to balance the capacitor dc voltage, measuring the capacitor voltage of each cell is required. The reference voltage v^*_{ref} for each cell is calculated from the averaged voltage of the capacitors, which is expressed as

$$v * ref = \frac{1}{N}\sum_{j=1}^{N} v * Cj \qquad (5)$$

As the cell capacitors are in the resonant operation, each capacitor voltage contains a considerable ac component. First-order low-pass filters are used to obtain the dc components of the capacitor volt-ages. As low-pass filters have to be implemented digitally, the transfer function of the filter can be written as

$$f_{LP}(z)=\frac{\alpha}{z-1+\alpha} \qquad (6)$$

with$\alpha = \omega cTb$, where $\omega c$is the cutoff angular frequency and Tb is the sampling period. By comparing the reference voltage to the dc voltage of each cell, a proportional feedback control is used for regulation. A dead zone is created to allow a small tolerance of voltage imbalance. A saturation is used to limit the adjustable duty-ratio range. As the series current is positive at each switching instant (or in average), current measurement is not necessarily required for voltage balancing. The capacitor volt-age can be charged by increasing the duty ratio of each cell slightly.

B. Step-Down DC Transformer

The proposed converter has inherent-balancing ability and therefore can operate using open-loop control. Regardless of the voltage drop of semiconductors and tolerance of the cell components, the ideal output voltage is proportional to the input voltage when the switching frequency is fixed. This gives the possibility of using the prop-osed converter as a dc transformer. The ratio between the output voltage and the input voltage is roughly determined by the number of cells. By increasing the number of cells, higher step-down ratio can be achieved. However, as explained in the previous section, the current stress will be further increased as a function of N. To achieve higher step-down ratio, isolation transformers can be used to increase the step-down ratio without increasing the series ac current.

C. Output Voltage Regulator

If the switching frequency is limited in a certain range for a practical application, the proposed converter may require a secondary dc–dc conversion stage to regulate the output voltage. This is a good solution for output voltage control. However, classic frequency controllers can be used for output voltage regulation without a secondary dc–dc conv-erter. Frequency controllers have limitations in many applications, but as a simple solution, they can achieve the requirement under some certain Circumstances.

D. Economic Analysis Example on Low-Power Application

This section shows an example of the real value of the proposed concept. The generally used the input-series-output parallel (ISOP) converter scheme with dual active bridges (DAB) is compared with the proposed converter scheme based on medium-voltage and low-power applications from the econ-omic point of view. Both systems operate as step-down dc–dc converters from 10 kV to 800 V with a power rating of 100 kW. For the ISOP converter, there are five series half-bridge modules on the input side and five parallel diode bridge modules on the output side connected via five isolation transformers. In contrast, the proposed converter has five series half bridge modules on the input side and one diode bridge on the output side. To Implement the converters, the parameters of the modules of the two converter schemes are listed.

As the input voltage is 10 kV, with five modules used, each module should withstand volt-age of more than 2 kV. The ABB HiPak IGBT half -bridge modules 5SNG 0250P330305, which can withstand 3.3 kV dc voltage are used. The current rating of each module is 250 A, which is the lowest current available in 3.3 kV HiPak product series. The

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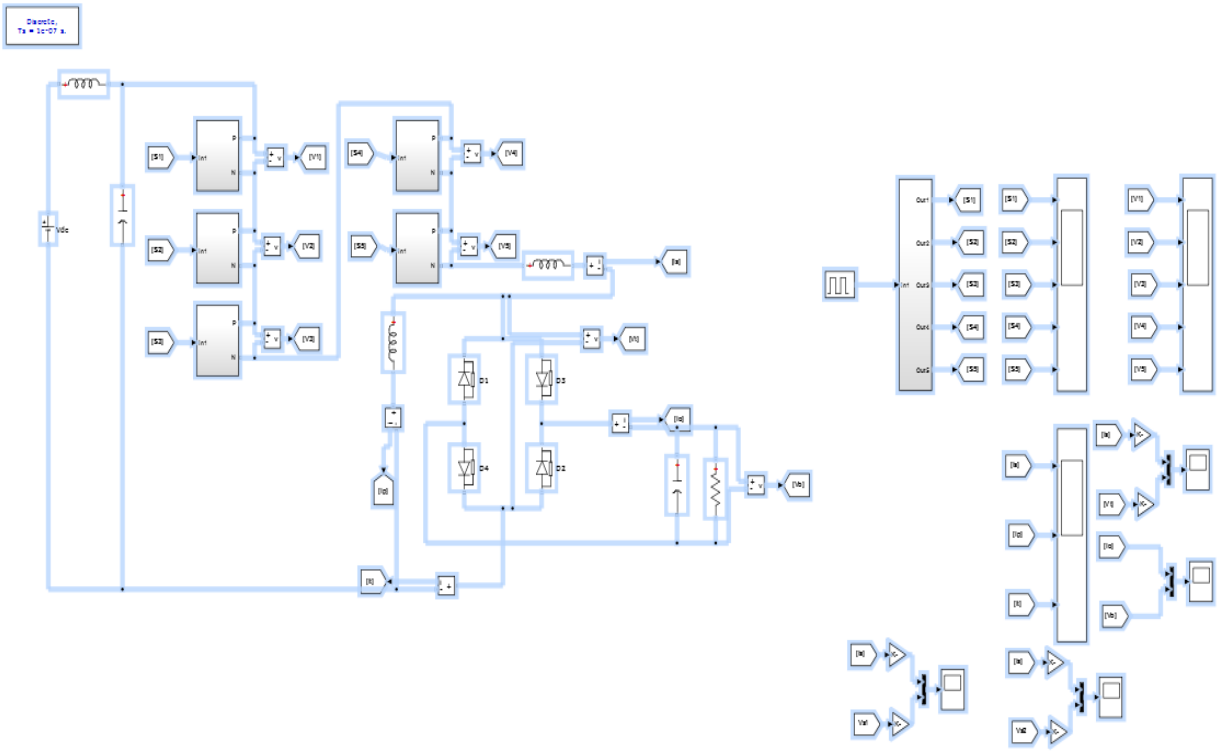
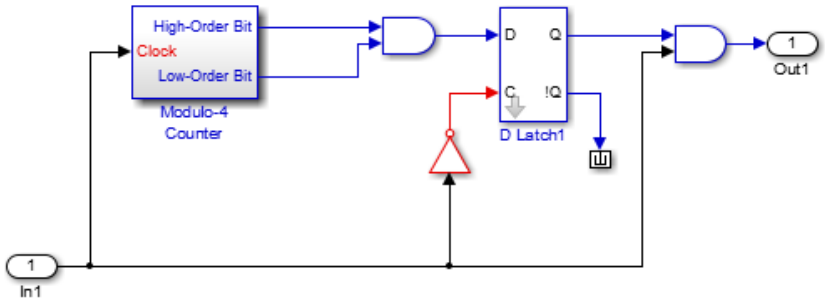
output side in both schemes has a voltage of 800 V and a total current of 125 A (equivalent to five parallel diodes with 25 A in each). Therefore, IXYS diodes (DSEP60-12AR) with the ratings of 1200 V and 60 A can be used. Compared to the cost of IGBTs, the cost of diodes is almost negligible. The ISOP DAB scheme uses five HiPak
IGBT modules with 10 A current flowing through each device, but the proposed scheme uses five HiPak IGBT modules with around 125 A current flowing through each device. The currents in both schemes are small enough compared to the 250 A device rating. Both schemes use the same numbers of semiconductor devices. On the other hand, the ISOP DAB scheme requires several bulky, heavy, and costly isolation transformers. Hence ,for this low-power (100 kW) application example, the proposed scheme exhibits obvious predominance compared to the ISOPDAB scheme in terms of cost and economy. However, for high power applicat-ions, the device current of the proposed converter will be much higher and IGBTs with high-current rating are required. Under such condition, the prop-osed converter will not be economic and efficient. It may be practical for high power applications in the future if the ratings of semiconductors are improved and the price is reduced. Compared to the ISOP DAB scheme, the proposed scheme has higher losses and higher device cost on the input voltage side. Nevertheless, the proposed converter does not require isolation transformers withstand-ding the entire input high voltage and operates with much higher frequency reducing the sizes of pass-ive components. There is one centralized rectifier used on the low-voltage output side. As a result, with the possibilities of semiconductor cost reduction, it provides a further option of implementing a high step-down ratio dc-dc converter comparable to traditional ISOP converters.

E. Simulation diagram



The above circuit explains the operation of MMC step down DC-DC converter with control circuit the sub circuit contains the logical circuit it gives pulses to the circuit



Generation of gate signals by using logical circuit

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Symbol	Quantity	Value
P	Rated power	250 W
V_{dc}	Nominal input dc voltage	500 V
v_o	Output dc voltage	45 V
I_{pk}	Maximum switch current	30 A
T_b	Sampling period	1 ms
L_{in}	Input filter inductor	9.8 mH
C_{in}	Input filter capacitor	840 μF
L_s	Series inductor	6.5 μH
L_p	Parallel inductor	3.3 mH
C_1	Cell 1 capacitor	57.9 μF
C_2	Cell 2 capacitor	69.1 μF
C_3	Cell 3 capacitor	58.2 μF
C_4	Cell 4 capacitor	57.7 μF
C_5	Cell 5 capacitor	57.8 μF
C_o	Output capacitor	3 mF

Table 1.PARAMETERS OF THE EXPERIMENTAL SYSTEM.

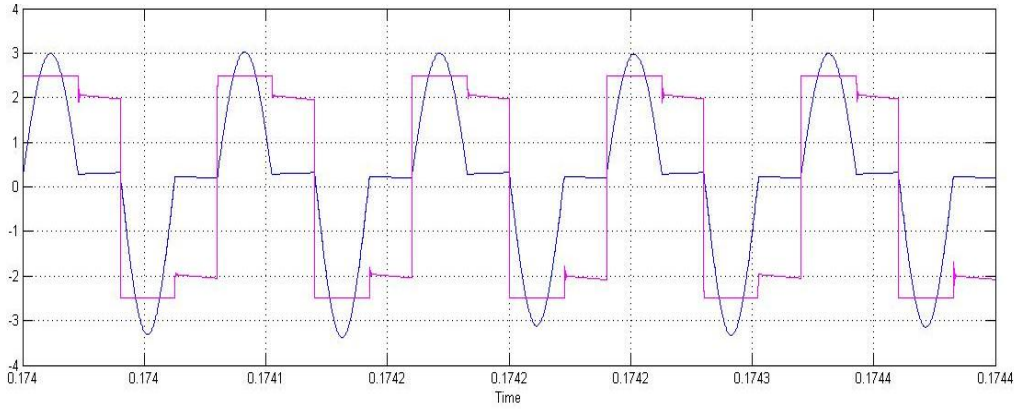

Fig.8(a). 2.5 kHz switching frequency.

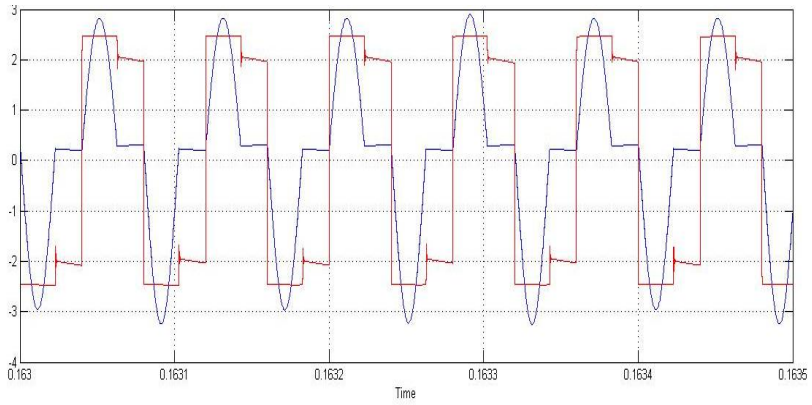

Fig.8(b). 3. kHz switching frequency.

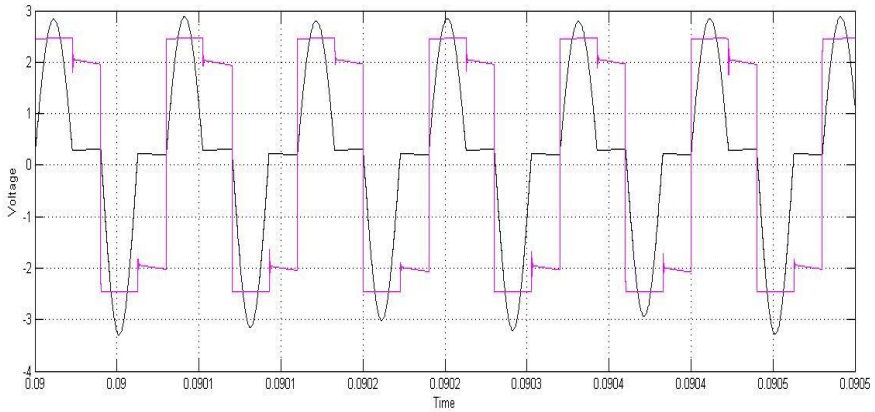

Fig 8(c) . At 3.5 kHz switching frequency

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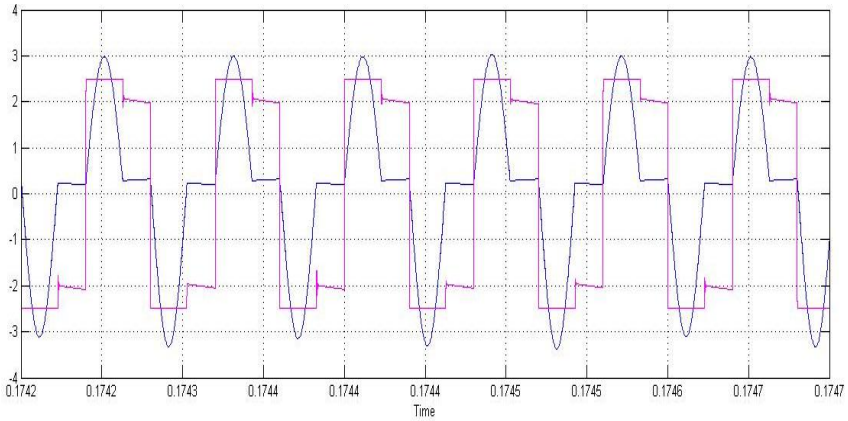

Fig 8(d) At 4 kHz switching frequency

Fig.8. Experimental waveforms under the open-loop condition (X–axis: Time, 20 μs/div, Y–axis: Magnitude of the rectifier input voltage: 20 V/div, and series current: 5 A/div)

5. TEST RESULTS

An experimental prototype was constructed based on the proposed circuit in Fig.1. with five half-bridge cells. The dc supply was rated at 500 V. Between the dc supply and the converter stack, an input *LC* filter was connected to suppress the ac current going to the dc supply. The filter inductance and capacitance were selected as 9.8 MHz and 0.84 mF, respectively. The half-bridge cells were implemented using capacitors with nominal capacitance value of 45 μF and IGBTs with PWM dead band of 5.3 μs. Note that big tolerance of capacitance applies during the manufacturing process. As a result, real values of the cell capacitors are different from each other. The switching frequency for each cell was chosen ranging from 2 to 4 kHz. Therefore, the operation frequency range was from 10 to 20 kHz. The nominal series resonant inductance was 4 μH and the parallel inductance was 3.3 mH. The capacitance of the output filter was 3 mF. The detailed circuit parameters are listed in Table1.

A. Open Loop Test

The proposed circuit has two different resonant frequencies *frp*and *frn*. With roughly measured Four typical switching frequencies were used for open-loop tests. The basic operation of the proposed circuit was tested without balancing con-trol or feedback control. The input dc voltage was 500 V. T parameters in Table I, the two resonant frequencies can be calculated as *frp*= 16.8 kHz and *frn*= 18.8 kHz, respectively. Note that the real resonant frequencies may be slightly different from the estimated values. However, this does not affect the operation principle of the converter. To show the typical waveforms, operating frequencies were chosen as 12.5, 15, 17.5, and 20 kHz to verify the design and analysis. Fig. 8 shows the open-loop controlled experimental waveforms of the rectifier input voltage and series current. When the equiva-lent operation frequency is smaller than both *frp*and *frn*,the series current resonates quickly and the rectifier input current becomes zero before both the ends of positive half-cycle and negative half-cycle. The converter is fully operating in the DCM [see Fig. 8(a)]. If the operating frequency is increased close to the first resonant frequency *frp*, the rectifier input current becomes zero at the end of the positive half-cycle [see Fig. 8(b)].However, as this operating frequency is still smaller than the second resonant frequency *frn*in the negative half-cycle, the rectifier input current becomes zero be-fore the end of the negative half-cycle, which can be observed in Fig. 8(b). Similarly, if the operating frequency is increased close to the second resonant frequency *frn*, it becomes higher than the first resonant frequency *frp*. The key waveforms can be seen in Fig. 8(c). In the positive half-cycle of Fig. 8(c), the series current resonates slower than the opera-ting frequency and the converter operates in the CCM. However, the rectifier input current reaches zero at the end of the negative half-cycle. The last experimental waveform in Fig. 8(d) shows that when the operating frequency is higher than both *frp*and *frn*, the converter operates in the CCM during both positive half-cycle and negative half-cycle. Under this condition, the series current peak is much smaller than that of the previous results and the stress on switches is much lower, but the turn-off currents of switches become much higher.

The voltages applied on the upper switch and the lower switch of a cell can be observed in Fig. 9. When the upper switch is ON and the lower switch is OFF, the voltage on the upper switch is Almost zero and the voltage on the lower switch is almost the cell capacitor voltage. Meanwhile, the cell capacitor is in the series resonant operation. Therefore, during this period, the voltage on the lower switch contains a higher ripple. On the contrary, when the upper switch is OFF and the lower switch is ON, the voltage on the upper switch is almost equal to the cell capacitor voltage and the voltage on the lower switch is almost zero. During this period, the cell capacitor is out of the series resonant

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operation ,and the voltage on the upper switch should be constant. It can be seen from Fig. 9(a), (c), and (e) that the upper switch off-time ripple is smaller than that of the lower switch in Fig. 9 (b), (d),and (f). Comparing Fig. 9 (e) and (f) to Fig.1, it can be seen that the theoretical wave forms and the experimental waveforms are in good agreement. The efficiency of the converter versus the switching frequency is shown in Fig. 10. The results were obtained under the same input voltage condition (500 V). It can be observed from the experimental results that the maximum efficiency is achieved when the switching frequency is over 3.5 kHz. Although the turn-off current [see Fig. 9(f)] is higher than that with lower switching frequencies [see Fig. 9(b) and (d)],the peak current is signify-cantly reduced. Lower conduction losses are therefore achieved resulting in lower total losses.

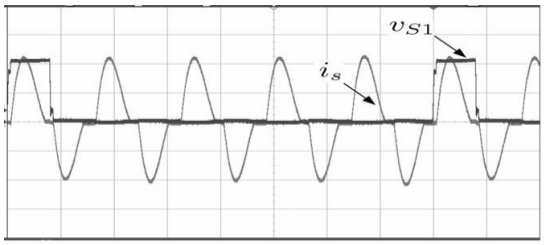

Fig.9(a).Upper switch voltage with 2.5 kHz switching frequency.

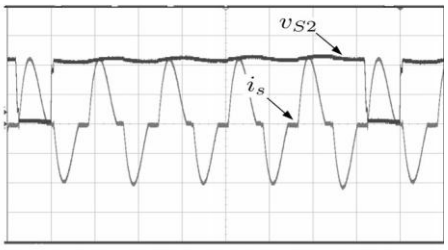

Fig.9(b). Lower switch voltage with 2.5 kHz switching frequency.

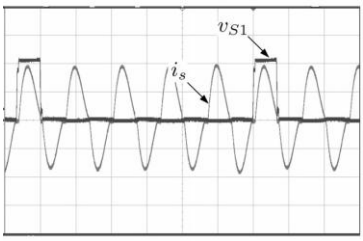

Fig.9(c).Upper switch voltage with 3 kHz switching frequency.

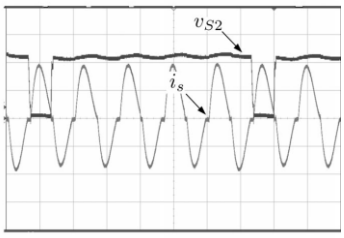

Fig.9(d). Lower switch voltage with 3 kHz switching frequency.

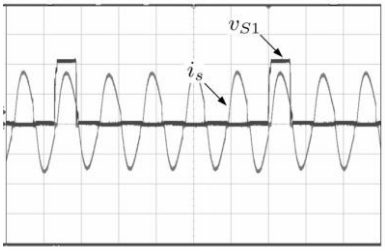

Fig.9(e).Upper switch voltage with 3.5kHz switching frequency.

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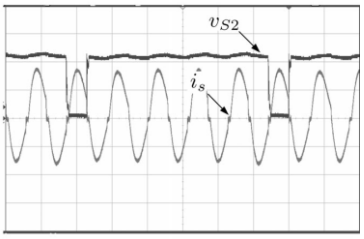


Fig.9(f). Lower switch voltage with 3.5 kHz switching frequency.

Fig.9.Experimental waveforms of switch voltages in Cell 1 under the open-loop condition (X–axis: Time, 50 μs/div, Y–axis: Magnitude of the cell switch voltage: 50 V/div, and series current: 5 A/div)

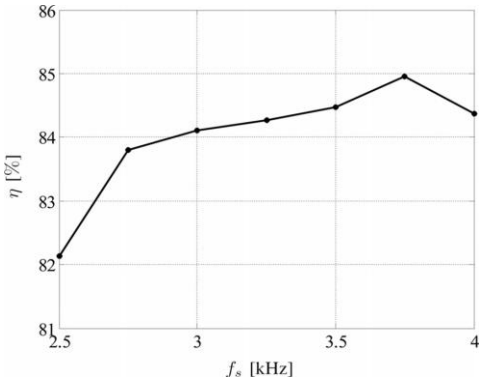
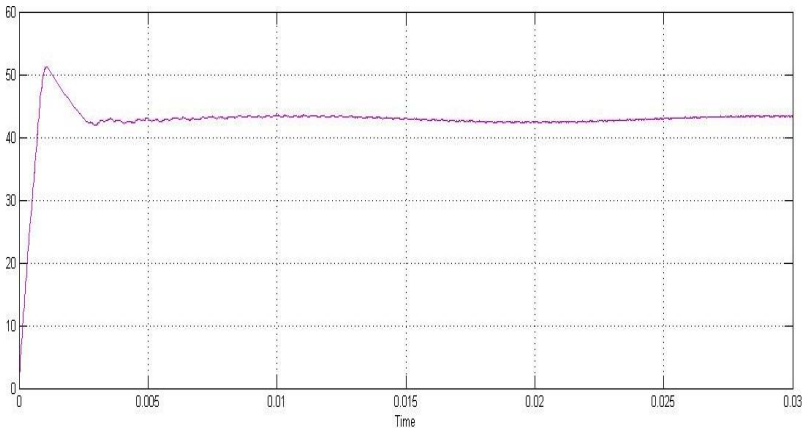


Fig.10. Efficiency versus switching frequency.



Output voltage wave form

B. Closed-Loop Tests

The closed-loop controller proposed in the previous section was implemented digitally. The converter was tested with a variable input dc voltage. The experimental results of a closed-loop capacitor balancing were compared to open-loop test results. It can be seen from Fig. 11 that without balancing control, the capacitor voltages of the converter are naturally balanced. In some applications, voltage sensors can even be eliminated from the converter for low-cost purposes. However, balancing control can be used to suppress the differences between the capacitor voltages. With closed-loop balancing control and frequency control, the experimental waveforms of the rectifier input voltage and series current are shown in Fig. 12. Note that the conduction losses are considerable when frequency changes, the output voltage regulation function is based on the open-loop experimental test results. When the input voltage changes, it can be seen that the frequency has been adjusted to maintain the output voltage around the rated value (45 V). To show the output voltage regulation, Fig.13 compares the output voltage of closed-loop tests with that of open-loop test results. It is shown that when the frequency controller is used, the output voltage changes slightly

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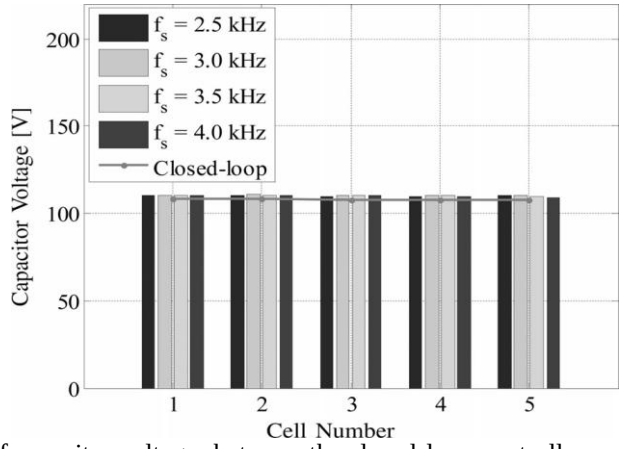

Fig.11. Comparison of capacitor voltages between the closed-loop controller and open-loop controller.

around the rated output voltage value. To achieve a more accurate output voltage for a wide input range, a lower ratio between *Lp* and *Ls* should be used. However, this may increase the maximum parallel current *ip*. A trade-off between output voltage regulation and power losses can be made to determine the inductance ratio [23]. A secondary converter can also be used to regulate the voltage level. The frequency voltage regulator of the proposed converter is only a simple solution suitable for some certain applications.

Fig.12. Experimental waveforms under the closed-loop condition (X–axis: Time, 20 μs/div; Y–axis: Magnitude of the rectifier input voltage: 20 V/div; and series current: 5 A/div) with (a) 480 V input voltage. (b) 520 V input voltage.

It is worth mentioning that the experimental tests were arranged simply to verify a concept design. For an input voltage of 500 V, the proposed converter is not the best solution. proposed converter may be more useful for high voltage applications where the modular multilevel configuration is necessary. For a practical application, detailed sizing and system design need to be considered [29].

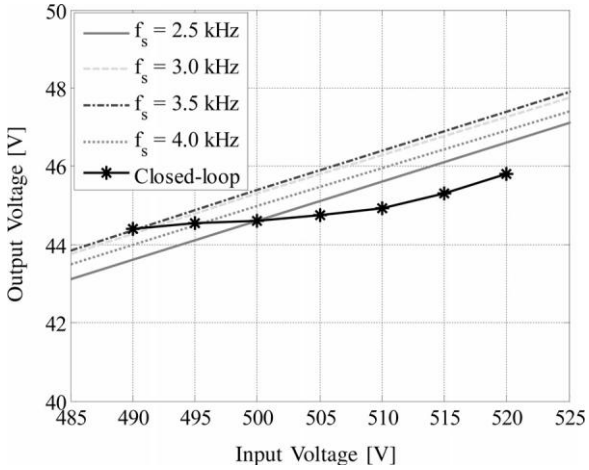

Fig. 12.Output voltage regulation of closed-loop controller.

Moreover, further studies need to be done on the balance between the cost and performance. The proposed converter should be carefully designed and compared to other options. The converter scheme used in practice should be chosen depending on applications to obtain a good tradeoff from the economic point of view.

6. CONCLUSION

As high step-down ratio dc–dc converters become increasingly interesting, there is a strong demand of novel dc–dc converter topologies. This paper has presented a new transformer less MMC dc–dc converter. The dc capacitors of the cells are used also for the resonant operation. The equivalent operating frequency can be increased as a function of the number of half bridge cells and the voltage step-down ratio is also dependent on the number of the cells. The proposed converter has a simple configuration and inherent-balancing capability. Two resonant operating frequencies exist in the converter. The converter can operate under open-loop control as a dc transformer. It exhibits a good linearity with

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different switching frequencies. When the closed-loop controller is used for the converter, the capacitor voltages are balanced and the output voltage is regulated within a smaller tolerance range of the rated value. Compared to the other topologies such as PETs, the proposed converter may exhibit more losses as a high ac current is flowing through the cells. However, the proposed converter can eliminate the use of transformers and even cell voltage sensors. Hence, the proposed converter has the feature of reliability, scalability, and simplicity which may be suitable for high-voltage and low-power applications.

7. ACKNOWLEDGMENT

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