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NAND Logic Implementation in Optical Domain using Four-Wave-Mixing

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Abstract: We have implemented ultra-speed NAND gate in Optical domain based on four-wave mixing Bragg scattering in a fiber which is highly non-linear. The results are obtained through taking different data inputs and different experimental set-ups.

Keywords: Opti-System, optical logic; NAND gate; Four- wave mixing; SOA.

I. INTRODUCTION

As communication data rates are continuing to increase day to day, latency, as well as energy, can be saved by avoiding electrical signal processing up to some extent and directly relying on digital signal processing in the optical domain. Particularly, relying on superfast optical logic gates in the digital signal processing (DSP) can very much improve the efficiency [1] of the system.

More particularly, all-optical logic gates can be used to select critical components such as flip-flops, adders, and devices for data encryption for large bandwidth networks. Among the available techniques to build optical domain logic gates, nonlinear processes are perfect due to their ultrafast operation. Universal logic gate (Nand Gate) can serve as a basic building block for all other logic gates. Our approach can be easily applied to high data rates and can be converted to on-chip waveguide platforms, possibly enabling high-speed cascaded logical operation integrated all-optical systems.

II. WORKING PRINCIPLE

FWM-BS is a superfast nonlinearity of third-order optical process comprising of four waves, in which a single pump photon (ω_{pump2}) and a signal photon (ω_{signal}) are interacted to obtain a pump (at a different frequency, ωpump1) and idler photon (ω_{idler}), as shown in Fig.1; energy conservation requires that

$$\omega_{pump2} + \omega_{signal} = \omega_{pump1} + \omega_{idler}$$

Due to the FWM-BS effect, low-noise frequency conversion [2, 3], translation of quantum states [4, 5], and optical isolation [6] have been demonstrated. Here, we utilize the FWM-BS process to demonstrate an all-optical domain NAND logic gate. The logical inputs are translated onto the two pump waves in the FWM-BS process, and the depletion of the continuous wave signal yields the NAND optical logic gate output.

Here in the below signal photon and a pump2 photon can be converted into a pump1 photon and an idler photon.

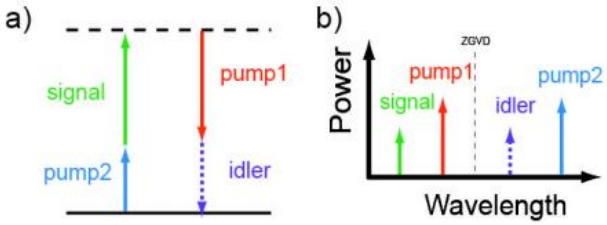

Fig 1 Energy conversion in FWM process

III. EXPERIMENTAL SETUP

The implementation of the NAND gate is depicted as shown in the Fig. 2, where the first part of the block diagram represents the process of FWM and if we have taken the output at the end of first BPF the output will be similar to the AND gate logic. Here two data signals are given as input to the first coupler and an output is obtained Which is of different wavelength and this output signal is passed through an EDFA amplifier .The output signal and pump signal will be given as input to the second coupler, the output is filtered through a BPF and again passed through an EDFA amplifier.

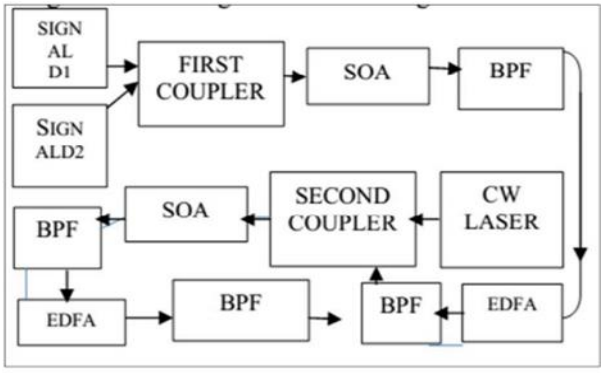

Fig. 2 NAND gate block diagram

The wavelengths assumed for the experimental set-up for D1=1548.7 nm, D2=1563.5 nm, pump signal=1540 nm and the output obtained signal consist of a different wavelength.

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The output results are depicted in the results section in the Fig. 4 output (where the input signal D1='0'.D2='1') and Fig. 5 output (where the input signal D1='1', D2='0').

Demonstrating the execution of the NAND logic function, the setup of experiment is shown Fig.3 is used. The phase modulator is used in place of an amplitude modulator, the two pumps are to be amplified separately by one EDFA, a 99/1 splitter is aligned before HNLF to monitor the pump power, and the output of the HNLF is sent through an OSA. The exact experimental setup is as follows: an 800-mHNLFwith zero group velocity dispersion (zGVD) wavelength at 1552 nm is used as the nonlinear element for the logic operation. The signal (1540.0 nm) and pump2 (1563.5 nm) are equally spaced in frequency from the zGVD wavelength of the fiber to achieve phase matching, and pump1 is set to 1548.7nm. The pumps and signal wave is generated with continuous-wave (CW) lasers. The two pumps are mixed by a 50/50 coupler. For the basic pump depletion measurement, the combined waves are to be phase modulated to suppress the stimulated Brillouin scattering (SBS) in the HNLF. The two pumps will be separated with a wavelength division multiplexer (WDM) and they are amplified by an EDFA for independent control of both polarization and delay and subsequently combined with the signal through a series of two WDMs for launching into the HLNF where the NAND logic gate operation occurs. The optical spectra are obtained through an OSA at the output of the HNLF .This set-up explained in Fig. 3 is used for the depletion ratio to the function of total input power are measured at first.

Fig. 3 shows the setup for FWM-BS NAND logic gate demonstration. An amplitude modulator (AM) is used to convert the logical inputs on each of the two pumps. A tuneable optical delay line (TODL) is deployed to match the bits of the two channel pumps, and the output of the HNLF is sent via a tunable filter and a photodiode to isolate the pumps and signal individually in the time domain, however, the details regarding the setup are described previously.

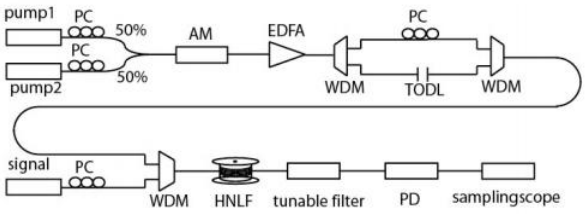

Fig. 3 Systematic sketch of experiment for NAND logic gate generation

To validate the NAND logic gate as a superfast all-optical logic function, time domain measurements are performed. In this case, an arbitrary pseudo-random binary sequence (PRBS) pattern is encoded onto each pump. The results of this demonstration are shown in Fig. 6. As is shown, the signal shows a low level (logic 0) when both pumps are at high levels (logic 1), while for all other cases the signal maintains a high output level (logic 1), thereby validating the NAND optical logic gate operation.

IV. OPTI-SYSTEM EXPERIMENTAL SETUP

The fig.4 represents the detailed internal block shown in the fig.2 and it can be explained as below:
The two PRBS are used for the bit sequence generators are used in the set-up. Here the PRBS generator and the continuous lasers are deployed in the set-up for the modulation purpose of one wavelength and same another one is taken which produces different wavelength. These two different wavelengths are sent through a coupler (50:50) where the output is generated using the four-wave-mixing phenomenon and the output that is generated is of a different wavelength.

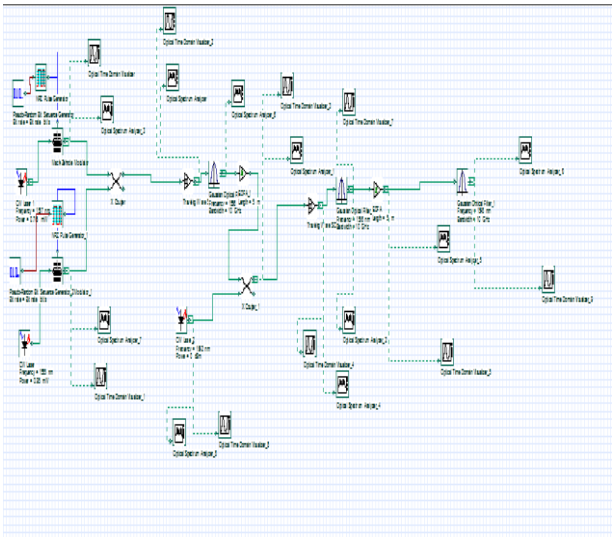

Fig. 4 Simulation set-up for the Nand gate logic for the above fig.2

The generated output signal and the pump signal are again are passed through a coupler where FWM process takes place in the set-up. Here the FWM process occurs only when the channel spacing is less that is we have to consider the wavelengths such that the FWM occurs. Hence, the output obtained signal is band pass filtered and the time domain visualizer is taken to observe the output.

The fig.2 shows the detailed simulation set-up for the fig.3 and it will be described as below:

First of all two pump signals of different wavelengths are considered and they were modulated and passed through a polarisation controllers and they were amplitude modulated and sent through a WDM multiplexer and passed through an optical fiber and then to a WDM demultiplexer, where the obtained wavelengths are separated onto the different channels, they were sent on the optical fiber. The demux output and another pump signal are given WDM multiplexer and the output is filtered through the Gaussian filter, it is observed on the optical time visualizer.

The parameters considered for each and every simulation block are shown in the set-up fig.4 and fig.5 respectively. The wavelengths that are assumed for the data signals and the pump signals are mentioned above in the explanation.

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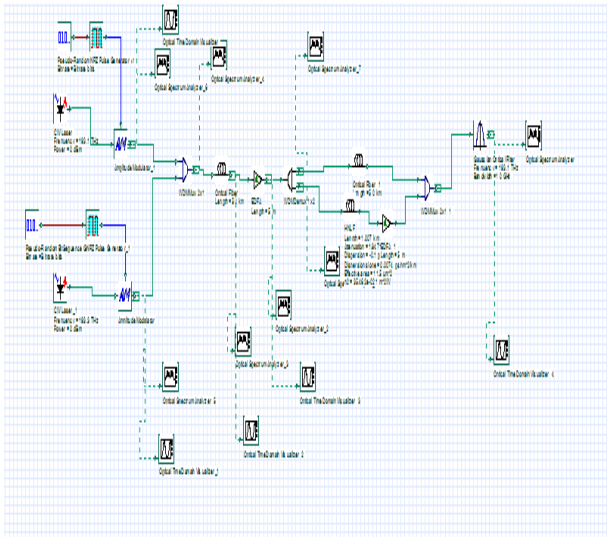

Fig5. Simulation set-up for the NAND gate logic for fig.3

V. RESULTS

In the fig.6 and fig.7 shown below is an output for the particular cases that are mentioned in the figure description. The fig.6 output is a case for the data signals D1=’0’, D2=’1’ and for the fig.7 the data signals D1=’1’, D2=’0’ are exclusively taken. When verified with NAND gate logic the outputs are satisfied.

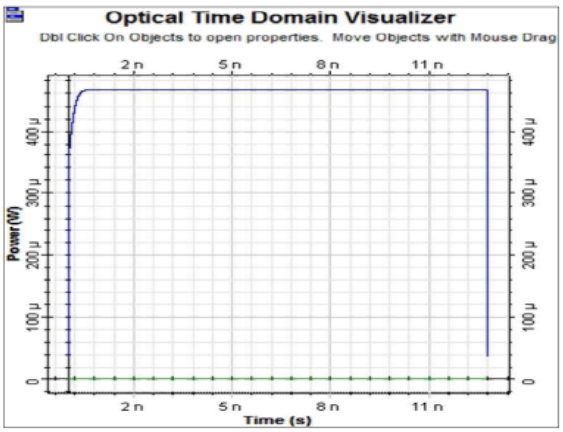

Fig 6. Time domain visualizer output D1=’0’, D2=’1’ showing signal Output high

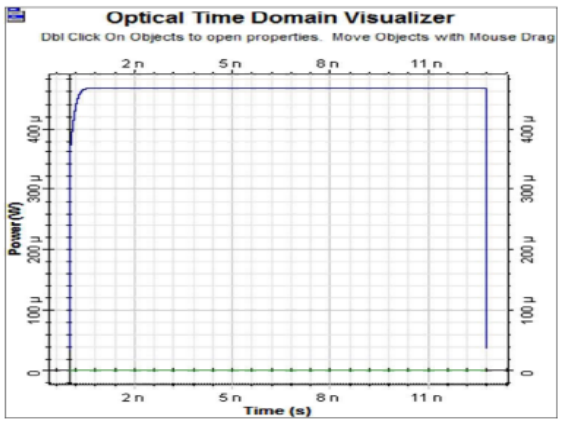

Fig. 7 Time domain visualizer output D1=’1’, D2=’0’ showing signal Output high

The output graphs are taken between time in seconds (X-axis) and power in watts (Y-axis) are considered. And it is verified for the other possible data signal combinations also.

The results shown in the below are the results obtained using the fig.3 where there are two pump signals and it will output obtained when passed through all the blocks that are present in the schematic sketch.

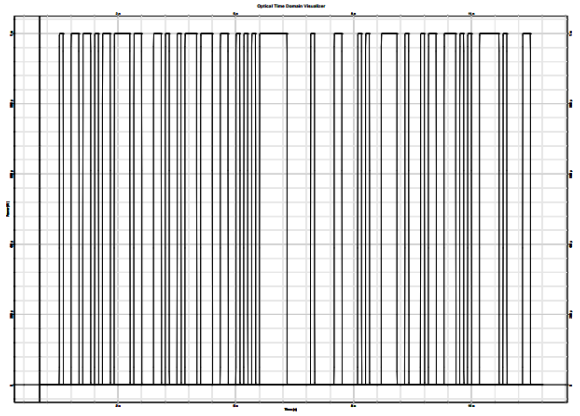

Fig. 8 Input signal as taken in pump 1

The graphs are plotted between the time taken in seconds (X-axis) and the normalized optical power (Y-axis).

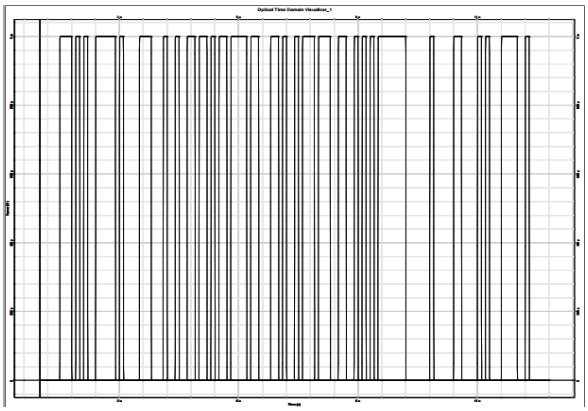

Fig. 9 Input signal taken as input at pump 2

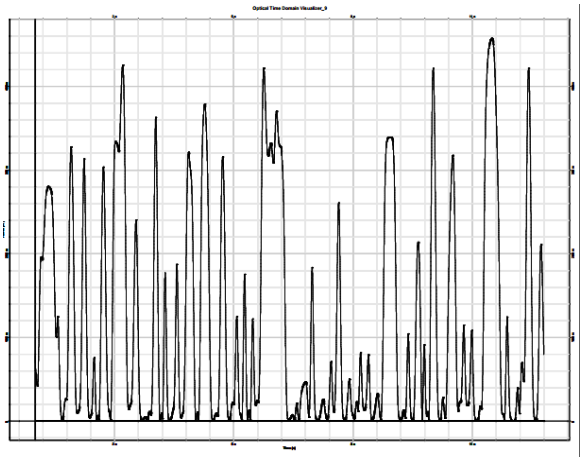

Fig. 10 Truth table of NAND gate at the output node

In the fig.8,fig.9,fig.10 we can see that all the possibilities of the NAND gate logic are verified.

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VI. CONCLUSION

In this paper, we demonstrate the first high-speed all-optical NAND logic gate, utilizing the FWM process in HNLF. This approach is directly extendable to high data rates and we anticipate that this method can be readily transferred to on-chip waveguide platforms, showing the promise for high-speed cascaded logical operation in integrated all-optical systems.

Here the taken signals that are taken are of different wavelengths and the wavelengths that we obtain at the output node are of different wavelength, this is due to the process of four-wave-mixing. This NAND gate logic can be used for parity bit generators, data encryption and header recognition.

This approach can be directly extendable to higher data rates and on-chip waveguide platforms. It promises fruitful fast speed cascaded operation in the integrated optical systems.

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