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Low-Power and Area-Efficient N-Bit Carry-Select Adder

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Abstract: Design of High Efficiency Carry Select Adder Using SQRT Technique presents many opportunities for increasing the speed and reducing the area of any data processor. Only Carry Select Adder (CSLA) is the fastest adders which are used in many data-processing processors to perform fast arithmetic operation. From the structure of the CSLA, it is clear that there is scope for reducing the area and delay in the CSLA. In this thesis, we have implemented a carry select adder for the computational process, these modules are programmed in VHDL Carry Select Adder (CSLA) is the fastest adder in all other adder. This work uses very simple and efficient gate-level modification to reduce the area and delay of the CSLA. Based on this modification 8-, 16-, 32-bit square-root CSLA (SQRT CSLA) architecture has been developed and it is compared with the regular SQRT CSLA architecture. The proposed design has reduced area and delay as compared with the regular SQRT CSLA with only a slight reducing the delay. This work evaluates the performance of the proposed designs in parameters that is delay, area, and their products with logical effort. The results analysis shows that the proposed CSLA structure is better than the regular SQRT CSLA.

Keywords: Carry Save Adder, Carry Select Adder, Ripple Carry Adder, and Binary to Excess-1 Converter, Square root CSA, and VHDL.

I. INTRODUCTION

In digital adders, the speed of addition is having the limitation by the time required to propagate a carry through the adder. Design of area and high-speed data path logic systems are one of the most important areas of research in VLSI system design. Addition widely the overall performance of digital systems and arithmetic function. In electronic system and applications adders are mostly used. Adders are used are multipliers, DSP to execute various algorithms like FFT, FIR and IIR.

Wherever concept of multiplication comes adders come in to the picture. As we know millions of instructions per second are performed in microprocessors. So, speed of operation is the most important constraint to be considered while designing multipliers. Due to device portability miniaturization of device should be high and power consumption should be low. Devices like Mobile, Laptops etc. require more battery backup. So, a VLSI designer has to optimize these three parameters in a design. These constraints are very difficult to achieve so depending on demand or application some compromise between constraints has to be made. Ripple carry adders exhibits the most compact design but the slowest in speed. Whereas carry look ahead is the fastest one but consumes more area. Carry select adders act as a compromise between the two adders. A carry-select adder can be implemented by using a single ripple-carry adder and an add-one circuit instead of using dual ripple-carry adders.

A multiplexer-based add-one circuit is proposed to reduce the area with less speed penalty. The sum for each bit position in an adder is generated serially only after the previous bit position has been summed and a carry propagated into the next position.

The CSLA is used in many calculation systems to avoid the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by Considering carry input Cin=0 and Cin=1 then the final sum and carry are selected by the multiplexers.

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and delay. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

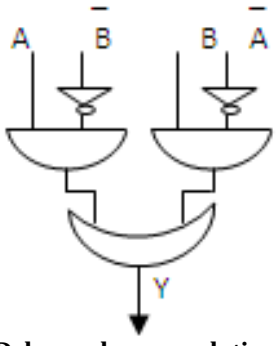

Fig 1: Delay and area evalution of XOR

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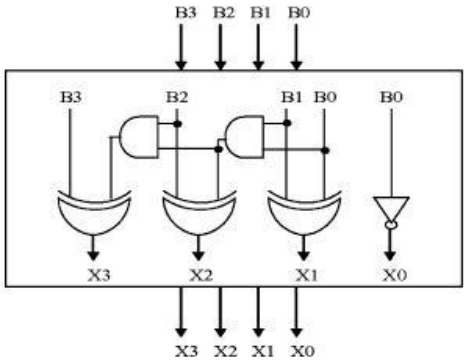

Fig 2: 4-b BEC

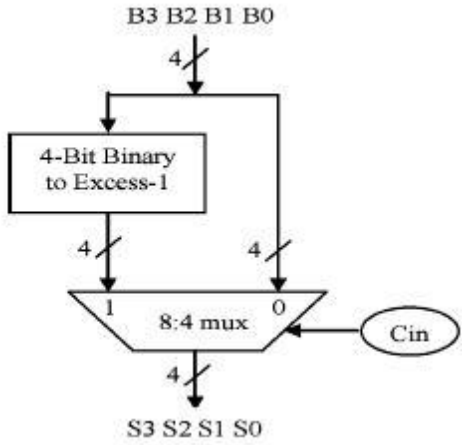

Fig3: 4-b BEC with 8:4 mux.

II. CARRY SAVE ADDER

A carry-save adder is one type of digital adder which is used in computer micro architecture for computational the sum of three or more n-bit numbers in binary. It is different from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of partial sum bits and another which is a sequence of carry bits. The carry-save unit consists of n full adders, each of which performs a single sum and carry bit based completely depends on the corresponding bits of the three input numbers.

Given the three n - bit numbers **a**, **b**, and **c**, it produces a partial sum **Psi** and a shift-carry **Sci**: sum can be performed by Shifting the carry sequence Sci left by one place, appending a 0 to the front (most significant bit) of the partial sum sequence Psi, Using a ripple carry adder to add these two together and produce the resulting n + 1-bit value. When adding together three or more numbers, using a carry-save adder followed by a ripple carry adder is faster than using two ripple carry adders. This is because a ripple carry adder cannot compute a sum bit without waiting for the previous carry bit to be produced, and thus has a delay equal to that of n full adders. A carry-save adder, however, produces all of its output values in parallel, and thus has the same delay as a single full-adder. Thus the total computation time (in units of full-adder delay time) for a carry-save adder plus a ripple carry adder is n + 1, whereas for two ripple carry adders it would be 2n.

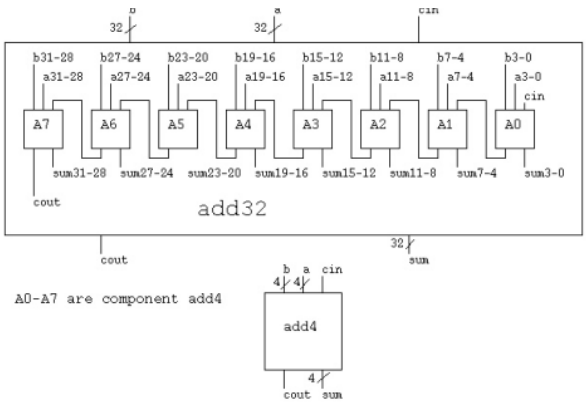

Fig 4: 32 bit carry save adder

III. CARRY SELECT ADDER USING RIPPLE CARRY ADDER

Arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates like AND, OR, NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication, subtraction or division .Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers. Each full adder inputs Cin which is the Cout of the previous adder. This kind of adder is **a** Ripple Carry Adder, since each carry bit "ripples" to the next full adder. The first full adder may be replaced by a half adder. The block diagram of 16-bit Ripple Carry Adder is shown here below32 Bit Carry Select Adder With Bec-1

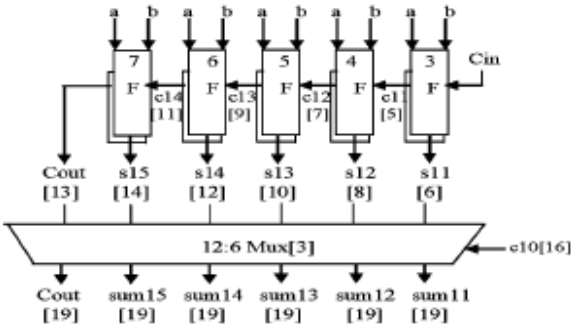

Fig. 5: Delay and area evaluation of regular SQRT CSLA F is a Full Adder.

The structure of ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic. In a 32-bit [ripple carry] adder, there are 32 full adders, so the critical path (worst case) delay is 31 * 2(for carry propagation) + 3(for sum) = 66 gate delays However, the

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CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1 then the final sum and carry are selected by the multiplexers The structure of the 32-b SQRT CSLA using RCA is 32 Bit Carry Select Adder With Bec-1 shown in Fig. It has five groups of different size RCA.

The delay and area evaluation of each group are shown in Fig. in which the numerals within specify the delay values, e.g., sum2 requires 10 gate delays The steps leading to the evaluation are as\ follows. 1) The group2 has two sets of 2-b RCA. Based on the consideration of delay values of the arrival time of selection input of 6:3 mux is earlier than and later than. Thus, is summation of and 2) Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA's. Thus, the delay of group3 to group5 is determined, respectively as follows: 3) the one set of 2-b RCA in group2 has 2 FA for and the other set has 1 FA and 1 HA for. Based on the area count, the total number of gate counts in group2 is determined. For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

IV. CARRY SELECT ADDER USING BEC-1

This structure is similar to regular 32-bit SQRT CSLA,the only change is that, we replace RCA with Cin=1 among the two available RCAs in a group with a BEC.This BEC can perform the similar operation as that of the replaced RCA with Cin=1.Fig shows the modified diagram 16-bit SQRT CSLA. The number of bits required for BEC logic is 1 bit more than the RCA bits. The modified block diagram is also divided into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and mux. First group contain one RCA which is having input of lower significant bit and carry in bit and produces result of sum (1:0) and carry out which is acting as mux selection line for the next group. The XOR gate in BEC of Modified CSLA is replaced with the optimized XOR gate in AOI of Modified Area Efficient CSLA .With BEC there is reduction of gates by replacing n bit RCA with n+1 bit BEC.

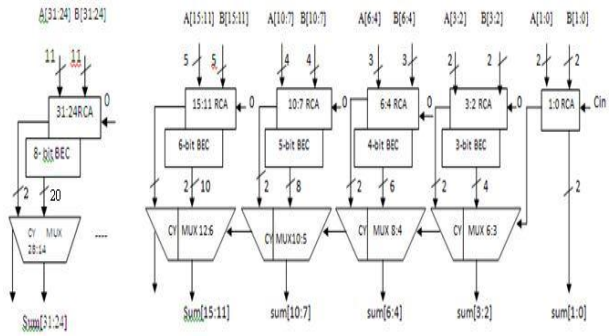

Fig 6: 32 bit Carry Select Adder using RCA AND bec-1

When the optimized XOR gate is used in Modified CSLA, it is verified that there is large reduction in number of gates. The MUX is used to select either the BEC output or the inputs given directly to a BEC circuit .In this design, the major function of MUX is to derive the adder speed.

V. DELAY, AREA EVALUATION METHODOLOGY OF CSA, CSLA USING RIPPLE CARRY ADDER AND CSLA USING BEC-1

Delay and area evaluation methodology of CSA, CSLA using ripple carry adder and csla using BEC-1 is shown in below table. In 32-bit CSA the area is increased as compared to regular csla and modified CSLA modified CSLA. In 32-bit SQRT CSLA moderate area is required as compared to CSA and CSLA using RCA. Delay is reduced by using 32-bit SQRT CSLA as compared to 32-bit CSLA using RCA.

The n 32-bit SQRT CSLA moderate area is required as compared to CSA and CSLA using RCA. Delay is reduced by using 32-bit SQRT CSLA as compared to 32-bit CSLA using RCA .The comparative values of areas shows that the number of LUT will be more for modified method for the 32-bit.

VI. RESULTS

The implemented Design of 32 bit SQRT CSLA has been simulated using VHDL. The 32-bit CSLA adder are designed and simulated using VHDL and the results are compared with CSA and Carry Select Adder using RCA.

After simulation the different size codes are synthesized using Xilinx ISE13.2i, Simulated files are imported into the synthesized tool and values of delay and area are noted.

VII. CONCLUSION

This paper proposed a simple approach to reduce area and delay of SQRT CSLA using BEC-1 architecture. The RCA with BEC in the structure is a great advantage to reduction in the number of gates and LUTs.

The result as shown in comparison table states that the modified 32-bit SQRT CSLA has a slightly large area for lower order bit which reduces for higher order bit and also delay is reduced to a great extent.

Thus the result shows that using modified method the area and delay will decrease so it is a good alternative for adder implementation in many data processors. Comparison table states that the modified 32-bitSQRT CSLA has a slightly large area for lower order bit which reduces for higher order bit and also delay is reduced to a great extent. Thus the result shows that using modified method the area and delay will decrease so it is a good alternative for adder implementation in many data processors.

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BIOGRAPHIES

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