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Design of Decimation Filter for Sigma-Delta A/D Converter

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Abstract: This paper introduces a kind of design method about the digital decimation filter design for Sigma-delta ADC with high performance, analyze its features of frequency and high pass filter, and give the results of simulation. The decimation filter can be applied to 1 bit, 128 times the rate of oversampling for Σ-Δ modulator, and can form a complete Σ-Δ A/D converter with Σ-Δ modulator. The area of this device is small, and the power consumption is very low with high precision. It can be easily realized with hardware in the SOC ASIC design and suitable for audio system.

Key Words: A/D Converter, Decimation Filter, FIR Filter.

1. INTRODUCTION

Generally there are many methods to design decimation filter, but conventional digital filter are designed by VLSI with DSP processor or FPGA structure. It has drawbacks with large sizes. With the development of electronic technology, some portable electronics device's bulk is more and more small, and it is impracticability for hardware's cost with large sizes. So it is beneficial to develop smaller size's filter than conventional digital filter. In addition, Σ-Δ A/D converter (D/A converter) trends to use higher frequency [1, 2], digital filters have indeed become the bottleneck of decreasing power consumption and area in the Σ-ΔA/D converter. So it is very important to optimize the power and the area [3,4,5,6]. This design is validated by MATLAB and gets a preferable frequency response.

The modulation function is achieved by analog circuit in Sigma-Delta A/D converter while subsequent signal is processed by digital circuit. Such a Modulator structure can utilize boundary conditions to optimize and design circuit topology with high performance and low power consumption data transfer. The Sigma-Delta structure can realize high precision A/D conversion, and more suitable for application in high speed digital circuits than other A/D converter in large scale integrated circuit. In order to meet more and more stringent requirements on power consumption and area for the general speech processing chip, in this paper the algorithm of decimation filter is optimized in the Sigma-Delta A/D converter, including the extraction technology and two levels FIR cascade.

At the same time, all levels of decimation filters are also optimized through filter design ToolBox in Matlab software. This design adopts the cascaded two times frequency FIR algorithm and CSD (Canonic Signed Digit) code filter coefficient to minimize the power consumption with reduced area and increased filter speed. In addition, according to the two channels A/D converter and two road extraction filter characteristics for speech stereo mode in the digital filter, the working frequency is set to two times sampling frequency (256 f_s). Two signals use the same set of hardware and left & right sound channel can share the same arithmetic unit conversion in different time, thus can further reduce chip area.

The Architecture of Decimation Filter

There are two major requirements for a decimation filter used in a Σ-Δ ADC [7,8]. The first is that the frequency response was designed to attenuate both out of band signals from the input to the ΔΣ modulator and the modulator quantization noise sufficiently to meet the overall ADC performance objectives. The second is that the decimation filter's truncation noise must be sufficiently low to allow the overall ADC performance to meet the required specification.

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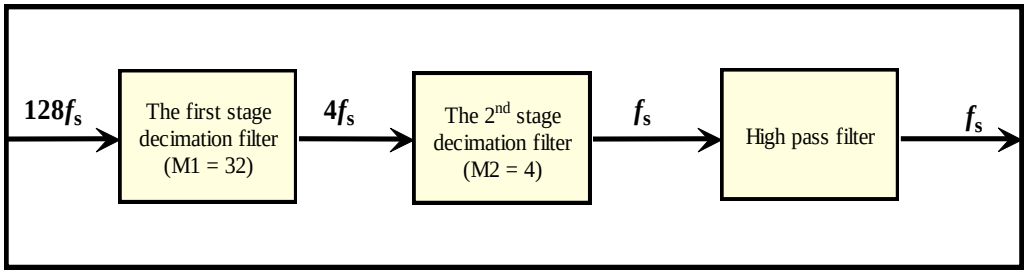

Fig1: Decimation filter architecture

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To efficiently perform the decimation and reduce power consumption, a two-stage decimation filter is used. The first stage filter decimates by 32 using cascade FIR comb filter, and the second stage filter decimates by 4 using 55th order FIR low pass filter. At the same time the second stage can compensate signal amplitude attenuation caused by the higher level. CSD technology can reduce filter coefficient on time-multiplier, thus can reduce area. In addition, an optional high pass filter is designed to filtering DC offset [9,10,11,12]. The digital decimation filter architecture used for this design is shown in Fig.1.

1.1 the First-stage Decimation Filter Design

The first stage filter accepts data at high sample rate, and performs the bulk of the decimation [13, 14]. Therefore, a simple structure is preferred to limit implementation size. Comb filters are an excellent choice for the first stage filter due to their simple implementation and good frequency response characteristics. In this design, a 4-order comb filter is designed to perform the decimation by 32. The transfer function $H_1(z)$ of this comb filter is

$$H(z)=\left(\frac{1-z^{-32}}{1-z^{-1}}\right)^4 \qquad (1)$$

General implementation of comb filters use the IIR-FIR structure [15], the comb filter is decomposed into two filters: an IIR filter $H_{11}(z) = [1/(1-z^{-1})]^4$ and an FIR filter $H_{12}(z) = [1-z^{-32}]^4$.

In this case, the power consumption of comb filters is very high. Using the commutative rule, the second filter is transferred after decimation, and then operates at a much lower sample frequency fs/32. To ensure stability, the minimum word length at the output of the IIR filter is fixed to $(1 + 4\log_2{}^{32}) = 21$ bits, where the number of bits at the input of this decimation filter is 1. The major drawback of this architecture is that IIR filter operates at maximum sample frequency fs and with a large word length. This increase drastically power consumption and limits the highest operate frequency of the decimation filter [16, 17, 18].

To decrease power consumption of comb filter, a multi-stage FIR filter is designed to implement comb filter in this design. Equation (1) can be written in the following form:

$$H(z)=\prod_{i=0}^{(\log_2 32)-1}(1+z^{-1})^4 \qquad (2)$$

Applying the commutative rule, we get the FIR2 structure shown in Fig.2 (c). In this structure, the Comb Filter is realized by cascading $\log_2{}^{32}$ (=5) identical FIR filters $(1+z^{-1})^4$, each decimating by 2. This structure has the advantage of no any stability problems and the word-length of each stage i limited to (1+4*i) bits and it is easy to implement decimation filters with programmable decimation ratio. Magnitude frequency response of 4th-order cascade FIR comb filter is in the Fig.3, which obtained by MATLAB tools.

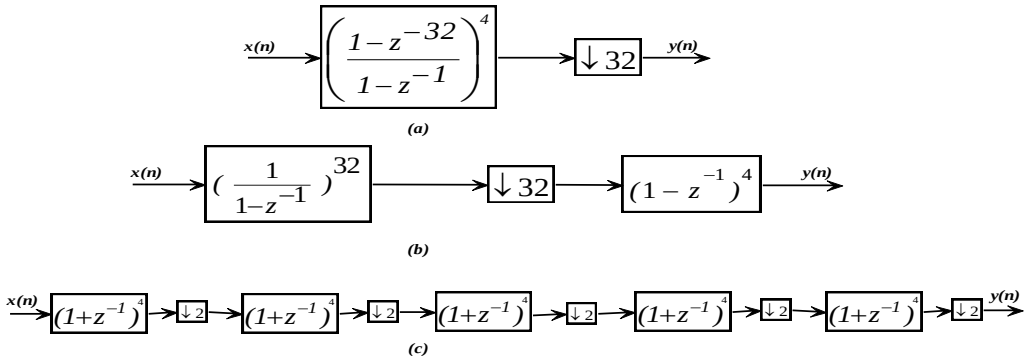

Fig.2: (a) Direct implementation (b) IIR-FIR implementation (c) Cascade FIR decimation by 2

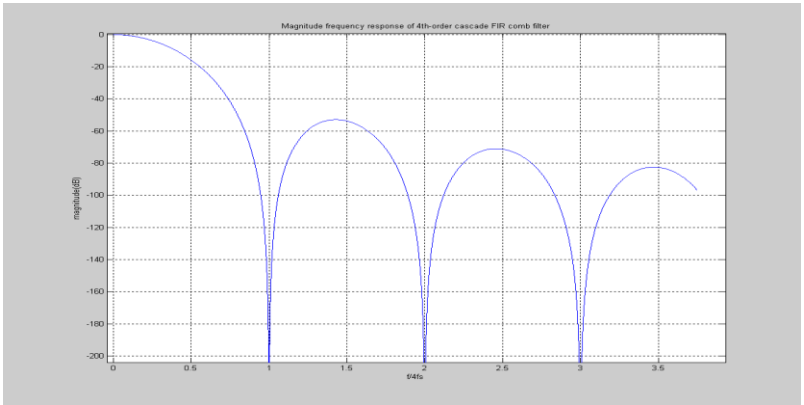

Fig.3: Magnitude frequency response of4th-order cascade FIR comb filter

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Note that the cascade of FIR comb filter results in a significant amount of in-band droop, which must be compensated for in the final stages of decimation.

1.2 the Second-stage Decimation Filter Design

The second-stage decimation filter performs the final decimation by 4 and compensates for the pass band droop of the first-stage decimation filter. A 56-tap FIR low pass filter is implemented as a poly-phase filter. This filter is presented by the difference equation:

$$y(n)=\sum_{k=0}^{55} h(k)x(n-k) \qquad (3)$$

Where h(k), k = 0, 1, 2, … 55 are the filter coefficients, x(n) is the input excitation, and y(n) is the output response. The filter coefficients h(k) of the FIR low pass filter in this design decide the performance of the filters. According to symmetry of FIR filter, h(k) = h(55-k), equation (3) could be written in the following form:

$$y(n) = \sum_{k=0}^{27} h(k)[x(n-k)+x(n-55+k)] \quad (4)$$

The coefficients h(k) is the design's keystone in which k from 0 to 27.

According to this design idea, we computed optimal coefficients h(k) and program to realize it by MATLAB tools. Fig.4 shows the magnitude frequency response of the 55th-order FIR low pass filter obtained by simulation. It has a -45dB attenuation for out of band signal and implements compensation for in-band droop in the first-stage decimation filter. Fig.5 shows the total magnitude frequency response and pass-band ripple of the cascade FIR filters.

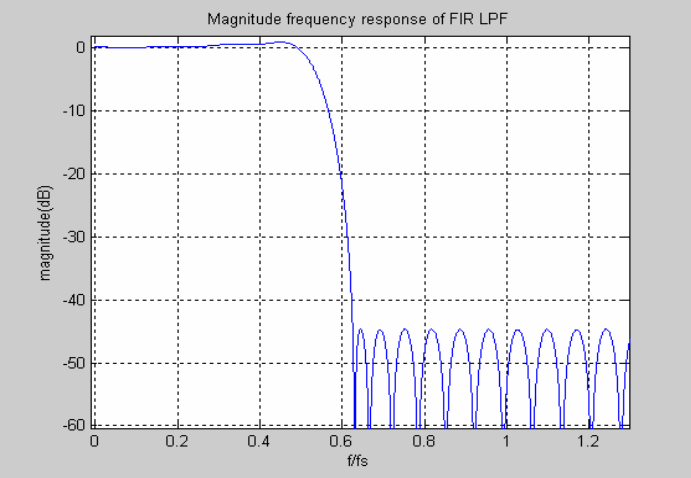

Fig.4: Magnitude frequency response of the 55th-order FIR low pass filter

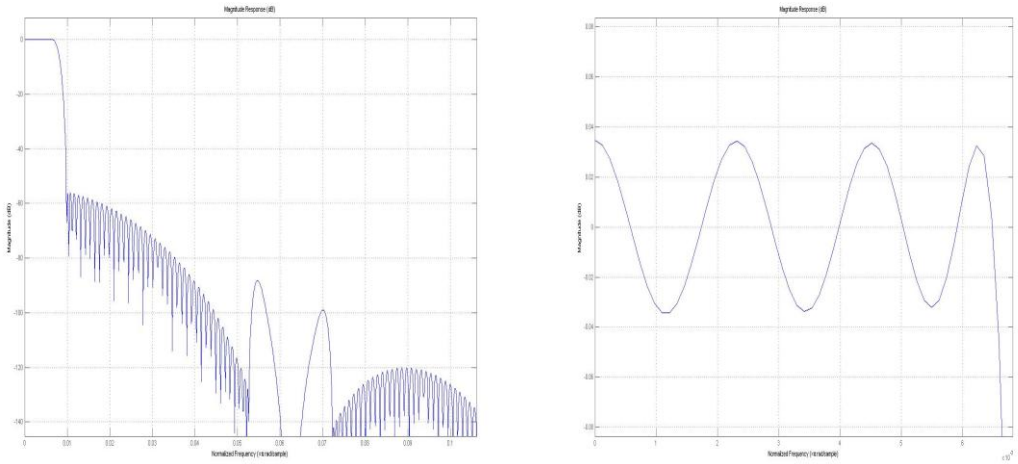

Fig.5: The total magnitude frequency response and pass-band ripple of the cascade FIR filters

1.3 the Digital High Pass Filter Design

Some DC offset can be produced by the modulator of Σ-Δ A／D Converter. DC offset will effect DSP compressed coding operation output by A/D converter, The digital high pass filter's design aim to eliminate DC offset.

The transfer function of the HPF is

$$H(z)=\frac{1-z^{-1}}{1-(1-\frac{1}{256})z^{-1}} \qquad (5)$$

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The cut-off frequency of the HPF is 25Hz at fs =48 kHz and also scales with sampling rates (f_s).

2. THE RESULT OF SIMULATION IN VERILOG HDL

The hardware program is achieved in Verilog HDL; the tool of simulation is NC Verilog. Table 1 describes the signals of the design. The simulation waveform is listed in Fig.6 and Fig.7.

3. CONCLUSION

In this design, a complete digital decimation filter design on Σ-Δ A/D converter is presented. This decimation filter gets a good frequency response which verified by software simulation and hardware test. The area of the device is 600um*590um in 0.13um SMIC technology.

Table 1: the Signal of Simulation

Signal	meaning
rst_n	Reset signal os the system
clk	The main clock of decimation filter
stereo	Enable signal for stereo
adcin_l	1-bit stream output by left channel of modulator
adcin_r	1-bit stream output by right channel of modulator
adc_lr	Left of right channel judgment signal
adc_dout	Ouput signal of decimation filter
adc_lr	Left channel output, high enable
adc_lr	Right channel output, low enable

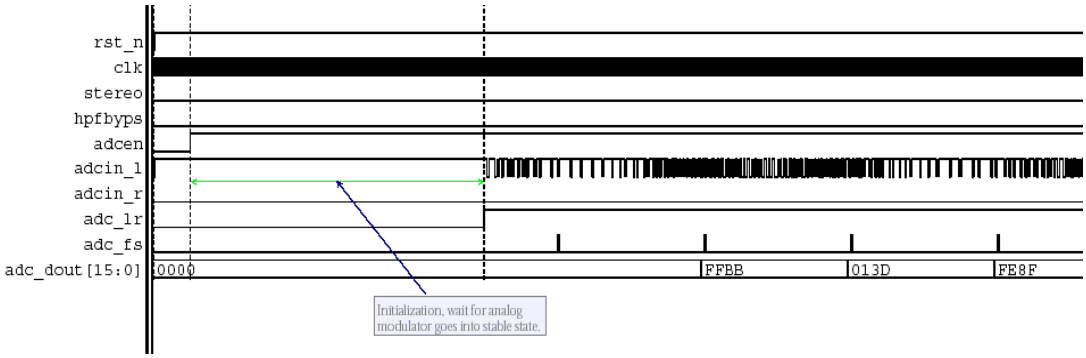

Fig.6: The simulation waveform of single channel

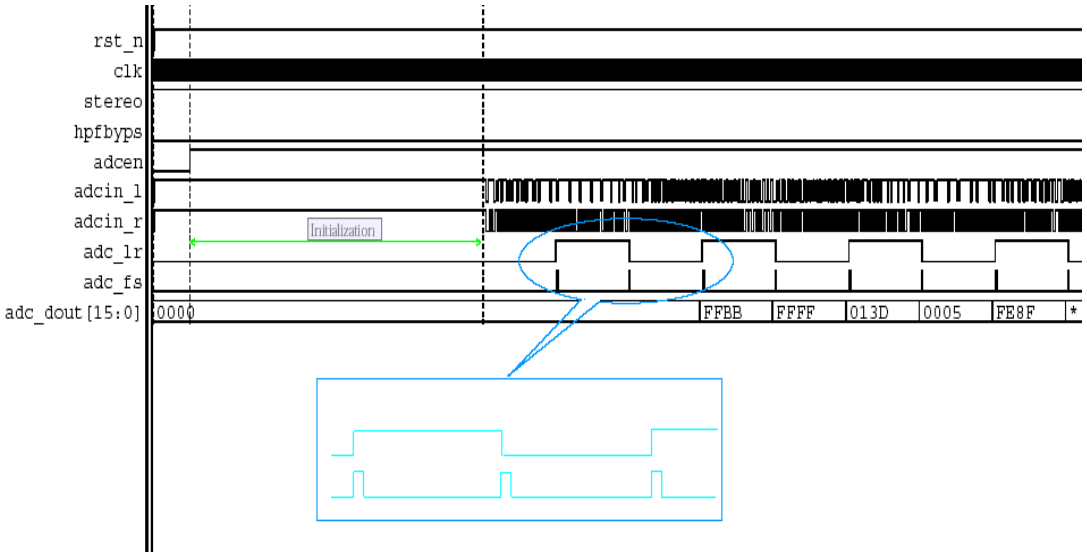

Fig.7: The stereo simulation waveform

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