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Advanced HVDC Systems for Renewable Energy

Swati Srivastava[1], Abhay Pratap Singh[2], Nav Bhushan Singh[3].

Assistant Professor, EE department, Greater Noida Institute of Technology, Greater Noida (Uttar Pradesh), India[1].

Abstract: The problem of stability has been a great concern. There are voltage stability problems and power stability problem which are of concern in the power system. The transient stability is a severe stability problem and is the major disturbance in synchronous alternator which can be reduced in many ways. This disturbance may cause severe problems. By using proper control strategies it is made sure that the synchronous alternator's rotor angle returns to a stable value after a sudden disturbance. In this project, HVDC links have been used in the IEEE 14 bus system and the difference of the voltage stability is seen in the system with and without HVDC links. Different control strategies have been implemented to solve the problem of transient stability.

The project is designed with the help of ETAP software where IEEE 14 bus system is built, load flow and transient analysis is done by applying the fault on bus 5 and bus 10. Then HVDC links are connected between bus 1 and bus 5, bus 9 and bus10. A fault is done on bus 5 and bus 10 and transient analysis have been done for both the faults. The results are obtained, compared and discussed in detail, which makes it clear whether transients are improved or not.

Keywords: Transient Analysis, HVDC link, Design, ETAP, Improvement, AC system

I. INTRODUCTION

There are many advantages of HVDC which makes it better and more preferred than AC. The connection to wind power source is easier with HVDC, The system can be interconnected even if the two systems have different frequency, and different types of sources can be interconnected.[1] Power from offshore area can be connected using HVDC. Islanding is possible in very easy way. [2]

There are various applications of HVDC which makes it a preferable choice than AC. Some of the applications are shown in the diagram below. [3]

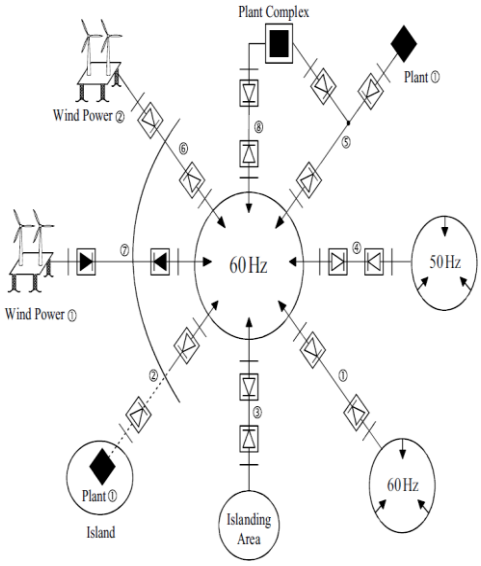

Fig 1 Application of HVDC

The choice of control strategy depends on the purpose for which it is used. The table below shows the control strategies used for different purposes.

Condition #	Desirable features	Reason	Control implementation
1	Limit the maximum dc current, I_d	For the protection of valves	Use constant current control at the rectifier
2	Employ the maximum dc voltage, V_d	For reducing power transmission losses	Use constant voltage control at the inverter
3	Reduce the incidence of commutation failures	For stability purposes	Use minimum extinction angle control at inverter
4	Reduce reactive power consumption at the converters	For voltage regulation and economic reasons	Use minimum firing angles

Table 1 Choice of control strategies used in dc links

II. MATERIAL AND METHODOLOGY

The current controller is basically a Proportional and Integral regulator. [4] As we all know the proportional part helps to give fast response with respect to the feedback and integral part is a slower part which used to make steady state error zero. The current error (Iorder - Idc) is send as input to the PI regulator. It gives out alpha order as output to the converter firing control. [5] Traditionally, rectifier will operate as current controller in order to have optimal operation point with reduced consumption of reactive power. Direct current is indirectly regulated by controlling the firing angle of the thyristor. The firing

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angle at rectifier station kept within a steady state range of ±2.5º by tap changer control. The ac voltage can be maintained constant by switching in and off of shunt capacitor and filter banks at nominal frequency. During steady state, current order Io from voltage dependent current order limiter (VDCOL) and measured dc current are same; hence the error of zero would be send to the saturated PI regulator in current control amplifier. In contrary, during transients Io would be varied as a function of dc voltage when the dc voltage hits the breakpoint of VDCOL, the error of Io and measured current will be sent to PI regulator with maximum limit and minimum limit. The max and min limit of CCA is determined by voltage control amplifier. The output from the PI regulator would be change in alpha order which is directly proportional to the change in current. [6]

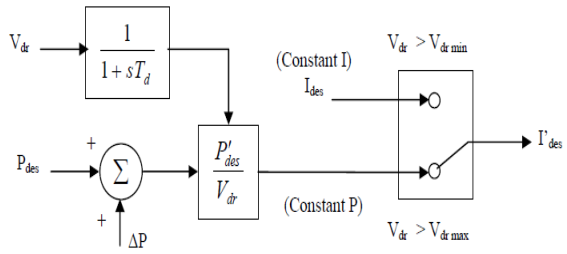

Fig 2 Control strategy used

III. DESCRIPTION OF THE MODEL

The diagram here consists of 14 buses. It is drawn based on the standard IEEE 14 bus system. Some of the parameters are changed according to the requirement and HVDC links have been connected between bus 5 and bus 1 and between bus 9 and bus 10. There are 5 generators with different generating capacity as mentioned below and 11 loads of different value and type as mentioned below.

	Capacity (MW)	Connected on Bus
Generator 1	232.5	1
Generator 2	40	2
Generator 3	0.01	3
Generator 4	0.01	6
Generator 5	0.01	7

Table 2 Table showing details of the generators connected

The loads chosen in the diagram include lumped loads as well as shunt loads. Lumped load is a combination of motor and static load; it is a constant impedance load. Description of loads is given in the table below.

	Connected on Bus	Real MW	Reactive MVar
Load 1	Bus 2	21.7	12.70
Load 2	Bus 3	94.20	19.00
Load 3	Bus 4	47.80	-3.90
Load 4	Bus 5	7.60	1.60
Load 5	Bus 6	11.20	7.50
Load 6	Bus 9	29.50	16.60
Load 7	Bus 10	9.00	5.80
Load 8	Bus 11	3.50	1.80
Load 9	Bus 12	6.10	1.60
Load 10	Bus 13	13.50	5.80
Load 11	Bus 14	14.90	5.00

Table 3 Details of load connected in the system

Total number of bus is 14 of the rating 1 kV each and there are three transformers of 100 MVA each between the buses. The impedance of the line is also visible in the diagram. Load flow analysis of the system with and without hvdc link has been done. The system with load flow is shown in the diagram below. In this diagram, the flow of real and reactive power is clearly drawn.

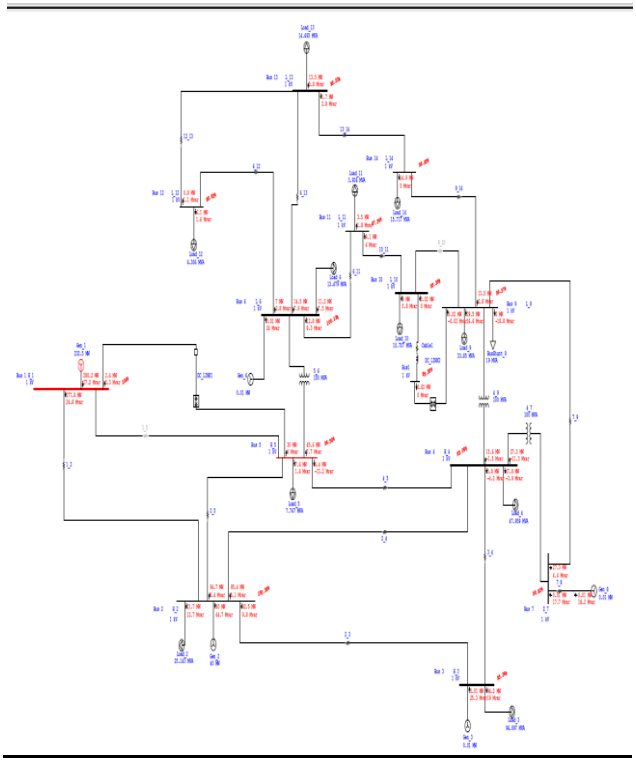

Fig 3 IEEE 14 bus system with HVDC links

IV. RESULTS AND DISCUSSION

The IEEE 14 bus system is subjected to a fault. The fault is created on bus 5 and the HVDC links connected between bus 5 and bus 2 is disabled. The bus voltage recorded at that point is as shown in the graph above. There is oscillation s in the system in the starting and after about 10 seconds also the transients occur. Therefore we can say that the system is not stable, it is not able to recover after the occurrence of the fault. Such system can lead to loss of synchronism and the system can get damaged as a whole. To remove such condition and

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obtain transient stability there are control strategies used in HVDC links connected between bus 5 and bus 2.

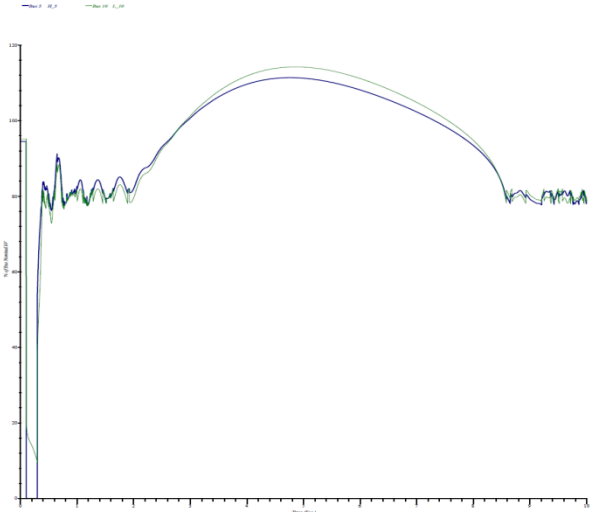

Fig 4 Voltage without any control strategy

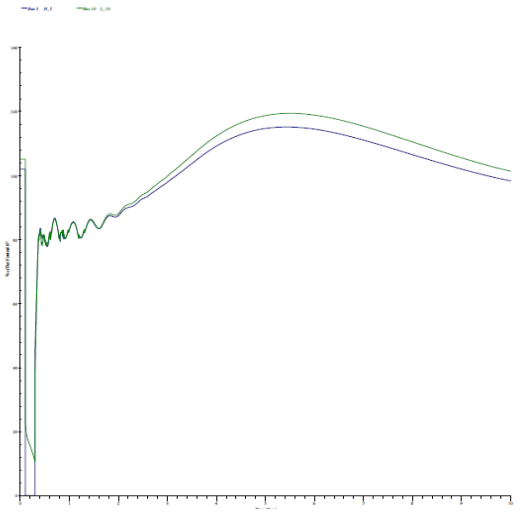

Fig 5 Voltage graph with control strategies implemented

The IEEE 14 bus system is connected with two HVDC links. One is between bus 5 and bus 2 and the other is connected between bus 9 and bus 10. The links are enabled now. The fault is created on the bus number 5 and control strategies are implemented so that there is more stable operation. On comparison with the graph of the system without HVDC control strategies, it is clearly seen that the system becomes more stable and the transients are improved after the initial disturbance.

Since this can be because of some chance therefore we need to confirm that the output of the system obtained is due to the control strategies applied in the HVDC link. This is why we have created one more fault on bus number 10 and applied control strategies to see whether the output obtained is similar.

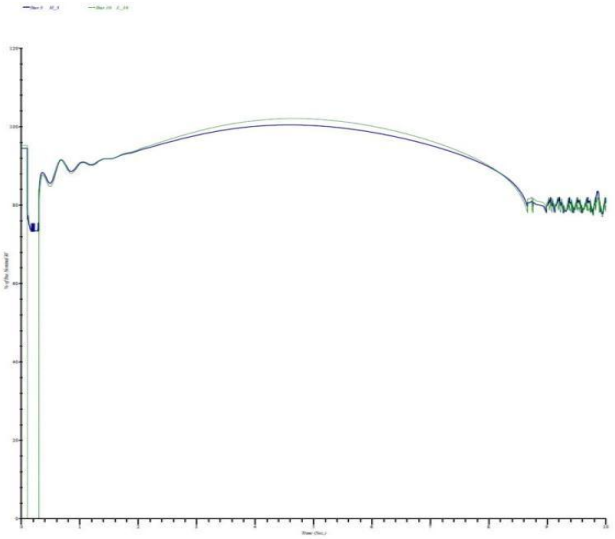

Fig 6 Voltage without any control strategy

The IEEE 14 bus system is subjected to a fault. The fault is created on bus 10 and the HVDC links connected between bus 9 and bus 10 is disabled. The bus voltage recorded at that point is as shown in the graph above. There is oscillation in the system in the starting and after about 10 seconds also the transients occur. Therefore we can say that the system is not stable, it is not able to recover after the occurrence of the fault. Such system can lead to loss of synchronism and the system can get damaged as a whole. To remove such condition and obtain transient stability there are control strategies used in HVDC links connected between bus 9 and bus 10.

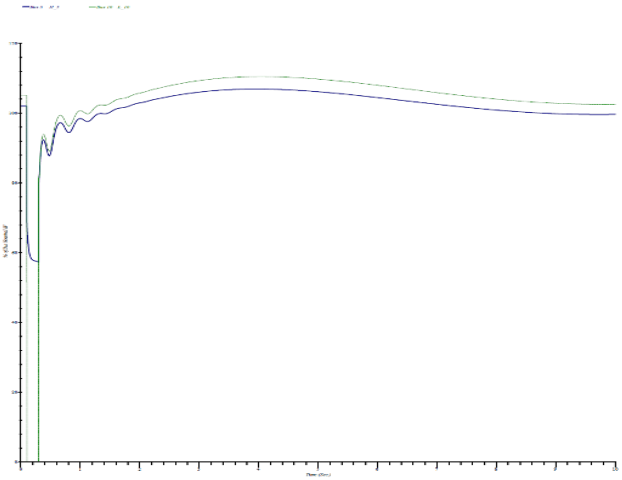

Fig 7 Voltage graph with control strategies implemented

The IEEE 14 bus system is connected with two HVDC links. One is between bus 5 and bus 2 and the other is connected between bus 9 and bus 10. The links are enabled now. The fault is created on the bus number 10 and control strategies are implemented so that there is more stable operation. On comparison with the graph of the system without HVDC control strategies, it is clearly seen that the system becomes more stable and the

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transients are improved after the initial disturbance. Now, there are two fault conditions which proves that by using control strategy in HVDC link, there is more stable operation and the transients are improved.

V . CONCLUSION

The project focusses on application of HVDC link in the AC system to improve the transient stability of the system. An IEEE 14 bus standard bus system is taken as a reference and some changes are done according to the requirement. HVDC link is connected between bus 5 and bus 2 and between bus 9 and bus 10. Load flow analysis is done for model with and without HVDC links. The project compares the results of the models with HVDC link and without HVDC link. Then a fault is created on bus 5 and bus 10. Then transient analysis is done on both the systems. There are different parameters whose graph is taken and an analysis is done on the voltage level of the two systems. There are different control strategies used in HVDC link to improve the transient stability of the system. The results of both the fault conditions have been compared with and without control strategy. There is clearly smoother graph of the system which is run with control strategy, there is improvement in the transients after the fault is cleared.

Event	Device ID	Time (sec)	Action
Fault	Bus 5	0.1	3-ph fault
Clearing of fault	Bus 5	1.8	Clear
Fault	Bus 10	0.1	3-ph fault
Clearing of fault	Bus 10	1.8	Clear

Table 4 Clearing time of fault without HVDC

Event	Device ID	Time (sec)	Action
Fault	Bus 5	0.1	3-ph fault
Clearing of fault	Bus 5	0.3	Clear
Fault	Bus 10	0.1	3-ph fault
Clearing of fault	Bus 10	0.3	Clear

Table 5 Clearing time of fault with HVDC

The result is compared on the basis of critical clearing time also. It is noted that the critical clearing time of the system with HVDC link is lesser than that without HVDC link. Therefore it can be concluded that by adopting different control strategies in HVDC link good improvements are obtained in transients of the AC system.

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