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Implementation of Tunable Current Amplifier and Voltage Amplifier using second generation Current Controlled Current Conveyor (CCCII).

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Abstract: In the field of analog VLSI design current mode devices have significantly gained importance. Current mode devices such as current conveyors have established their identity as the most demanding devices in the signal processing area due to their high bandwidth , greater linearity , larger dynamic range ,low power consumption , simple circuitry and occupy less chip area. The presented approach over here is to design current amplifiers and voltage amplifiers using current controlled current conveyor (CCCII). The second generation current controlled conveyor (CCCII) has the advantage of electronic adjustability over the CCII i.e. in CCCII; adjustment of the X-terminal intrinsic resistance via a bias current is possible. The CCCII has been designed to work both as current amplifier and voltage amplifier. Various simulations have been carried out to obtain the desired results. The outcomes show good results and an amplified waveform has been obtained in both the cases.

Keywords: Analog integrated circuits–current conveyor, Current controlled current conveyor (CCCII), Current amplifier, Voltage amplifier.

I. INTRODUCTION

In the recent field of analog integrated circuits current mode has been the most promising technique in VLSI design. This stems from its inherent advantages of wide bandwidth, high slew rate, low power consumption and simple circuitry. It has proven as a most capable technique that can help applying various design considerations which are ineffective at other design levels. Because of its superiority over the voltage mode approach, [1], the CM design approach appears to be a most suitable candidate for the next generation of analog VLSI.

Current mode design approach is one where circuits are operated on current and also the states of the circuits are represented in terms of currents rather than in terms of voltages. Current mode approach has numerous remarkable features, like, superior bandwidth, higher speed and better operational accuracy. Current mode design technique offers voltage independent high bandwidth analog circuits and current mode circuits are being widely used in high frequency circuit design applications. Current conveyor (CC) first introduced in 1968 [l] is commercially available now and has emerged as extremely versatile analog building blocks. It does not require highly sophisticated designs as demanded by the good performance VM amplifiers.

Further, this approach can also manage with comparatively low precision design components. The CM design approach has been successfully applied to a variety of circuit applications.

Current conveyor is a versatile current mode circuit, gaining acceptance as both a theoretical and practical building block. The current conveyor, with one high impedance input , one low impedance input and two with high impedance output is a suitable element for both voltage-mode and current-mode circuits. A current conveyor is four (possibly five) terminal device which when arranged with the other electronics elements in specific circuit configurations can perform many useful analog signal processing functions[2].In many ways the current conveyors simplifies circuit design in much the same manner as the conventional operational amplifier.

The current conveyor is receiving considerable attention as they offer analog designers some significant advantages over the conventional op-amp.

These advantages can be pointed out as follows:

1. Improve AC performance with better linearity.
2. Wider and nearly constant bandwidth independent of closed loop gain.
3. Relatively High slew rate.
4. Flexibility of driving current or voltage signal output at its two separate nodes, hence suitable for current and voltage mode devices.
5. Reduced supply voltage of integrated circuits.
6. Accurate port transfer ratios equal to unity hence employed in low sensitivity design.
7. Requirement of smaller number of passive components to perform a specific function.

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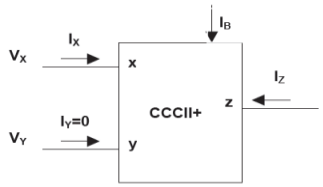
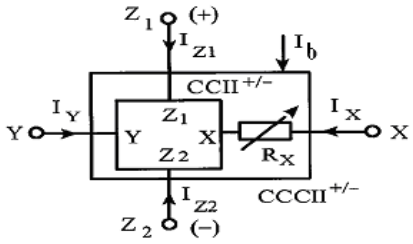
II. DESCRIPTION OF CURRENT CONTROLLED CURRENT CONVEYOR (CCCII)

Fig. 1 and Fig. 2 show the symbol and equivalent circuit of the second generation Current Controlled Conveyor (CCCII). A CCCII-based circuit, whether positive, negative or dual output [3, 7], provides electronic tunability and wide tunable range of its resistance at X-terminal [6]. The CCCII requires no external resistors; hence it is very suitable in the design of integrated filters and oscillators. Also, as the CCCII is current controlled current source, the CCCII based circuit is very suitable for high frequency operation. These features are very attractive to circuit designers [4].



(a)



(b)

Fig. 3.1 (a) Block diagram of CCCII+

(b) Equivalent Circuit Diagram of CCCII

The relationship between the voltage and current variables at input and output ports X, Y and Z of the CCCII can be expressed by the following matrix,

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

where the sign ± refers to plus-type or minus-type CCCII, respectively, and RX denotes the intrinsic resistance at X terminal. R_X is adjustable by a supplied bias current I_b which can be expressed through a class AB trans-linear loop, which is used as input section.

$$I_Y = 0 \qquad (3.1)$$

$$V_X = V_Y + I_X R_X \qquad (3.2)$$

$$I_{Z+} = I_X \qquad (3.3)$$

$$I_{Z-} = -I_X \qquad (3.4)$$

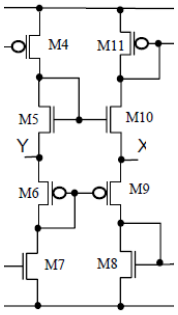


Figure 3.2 Translinear loop of the circuit in fig 3.3

The characteristics of the above given fig 3.2. An estimate of the impedances at node X and Y can be as follows[8]:-

$$Z_X \cong \frac{1}{gm_{10}+gm_9} \cong \frac{1}{gm_{10}+g_{m9}}$$

$$Z_Y = r_{07} || r_{04}$$

Refer from fig. 3.2

$$Z_Z = \frac{r_{012} r_{013}}{r_{012} + r_{013}}$$

The voltage characteristics is

$$\alpha = \frac{1}{1 + \frac{1}{(g_{m10}+g_{m9})(r_{010}||r_{09})}} = 1$$

and

$$\beta = 1 \text{ when } (g_{m11} = g_{m12} \text{ and } g_{m8} = g_{m13})$$

voltage gain of the amplifier is the amplitude ratio of the output voltage to the input voltage.

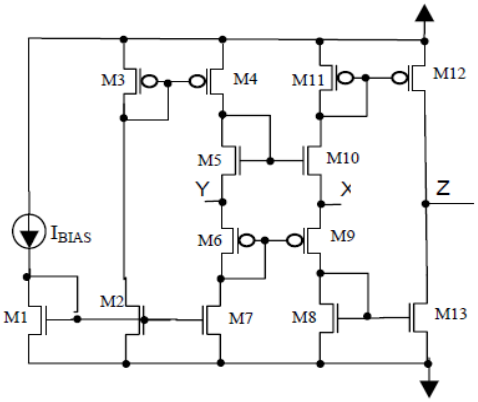
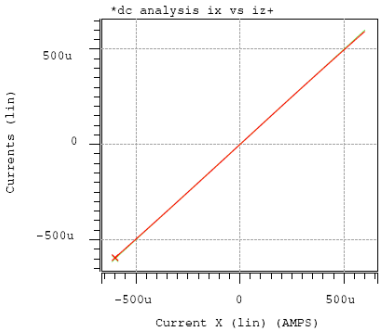


Figure 3.3: CMOS version of the CCCII+ realization.



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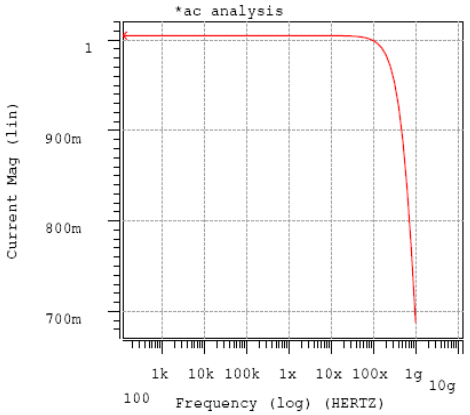

III. TUNABLE VOLTAGE AMPLIFIER

An electronic circuit whose function is to accept an input voltage and produce a magnified accurate replica of this voltage as an output voltage.

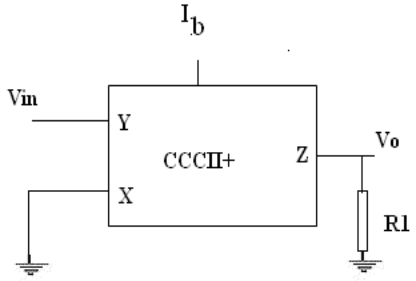

Fig.4.1 Circuit of Tunable Voltage Amplifier

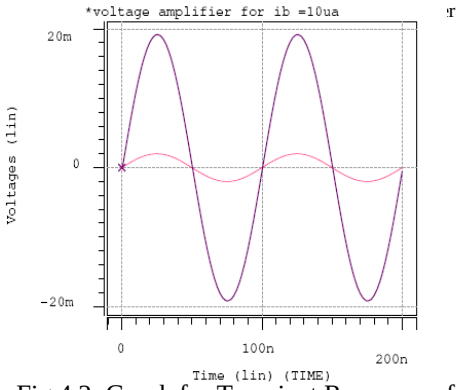

Fig 4.2: Graph for Transient Response of Amplifier for f=10MHz

The analysis of the amplifier circuit [9] shown in fig 4.1 is as follows

We know for CCCII+

$$V_Y = V_X + I_X R_X \quad (4.11)$$

Since $V_X=0$, $V_Y=V_{IN}$

$$V_0 = I_Z R_1 = I_X R_1 \quad (4.12)$$

$$V_0 = V_{IN}(R_1/R_X) \quad (4.13)$$

Where R_X depends on bias current I_b.

For realization, of the above voltage amplifier, CMOS design of CCCII+ is adopted, and the voltage amplifier of fig 4.1 is simulated on HSPICE .the input voltage is applied at node Y of the CCCII+ of the magnitude of 4mV peak to peak. The output is seen on Z+ node of the conveyor. The bias current I_b is taken as 10µA.The simulation results of the voltage amplifier are presented in fig 4.2. The output obtained after the simulation is of value 38.4mV (peak to peak). The output is seen on Z+ node of the conveyor. The bias current I_b is taken as 10µA and theoretically 10 is selected as the gain of the voltage amplifier. The simulation results of the voltage amplifier are presented in Fig 4.2. The output obtained after the simulation is of value 38.4mV (peak to peak) that means the practical value of gain is 9.6.

Figure 4.3 given below shows the frequency response of the above mentioned amplifier. AC analysis is performed to know about the bandwidth which is an important parameter and can be determined as the frequency at which the power of the load is at least 50%.This condition in absolute units corresponds to 70.7% and 3 dB in decibels units.

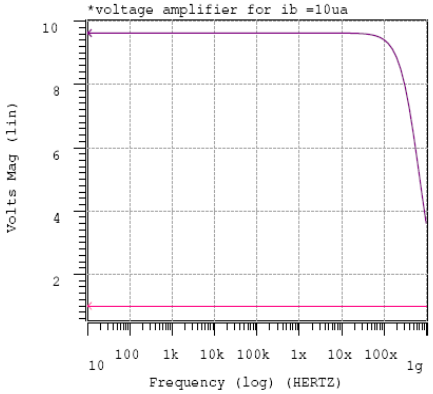

Fig 4.3: Frequency Response of Amplifier

The graph shown below in figure 4.4 is plotted across the voltage gain to the device bias current in µA . As can been seen from the graph that the voltage gain increases with the increase in device bias current I_b. As bias current varies from 0µA to 100 µA, voltage gain increases from 1.1 to 1.8.

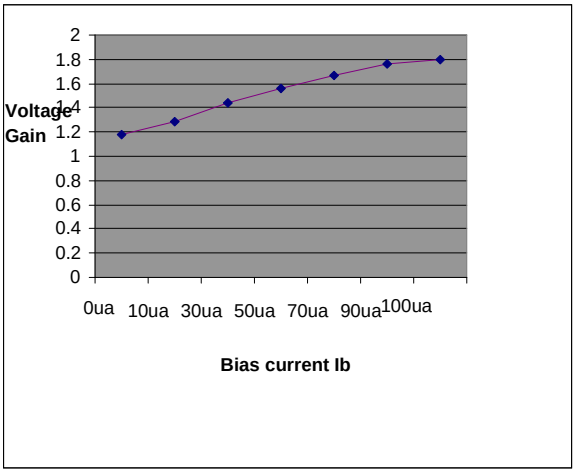

Fig4.4 Graph between Voltage Gain & Bias Current, R1=1K const

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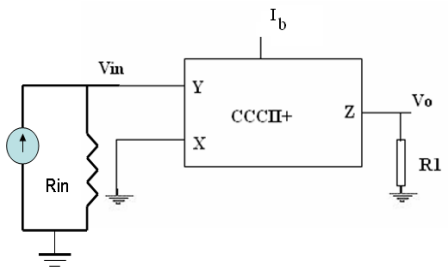
Fig.4.5 Circuit of Tunable Current Amplifier



The analysis of the current amplifier circuit [10] shown in fig 4.5 is as follows

We know for CCCII+

$$V_Y = V_X + I_X R_X \quad (4.21)$$

Since $V_X=0$,

$$V_Y = I_X R_X = I_{IN} R_{IN} \quad (4.22)$$

$$I_X = I_{IN} R_{IN}/R_X = I_Z \quad (4.23)$$

$$\text{Current Gain } A = I_Z/I_{IN} = R_{IN}/R_X \quad (4.24)$$

For realization, of the above current amplifier, CMOS design of CCCII+ is adopted, and the current amplifier of fig 4.5 is simulated on HSPICE .

The input current is applied at node Y of the CCCII+ of the magnitude of 2µA peak to peak. The output is seen on Z+ node of the conveyor. The bias current I_b is taken as 10µA.

The simulation results of the current amplifier are presented in fig 4.6. The output obtained after the simulation is of value 18.8 µA (peak to peak).

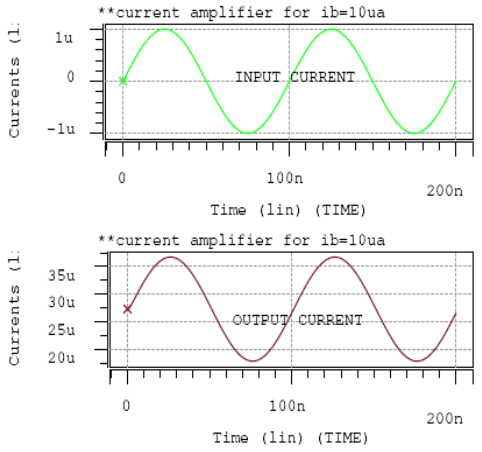


Fig 4.6 Transient analysis for current amplifier

Figure 4.7 given below shows the frequency response of the above mentioned amplifier. AC analysis is performed to know about the bandwidth which is an important parameter and can be determined as the frequency at which the power of the load is at least 50%.

This condition in absolute units corresponds to 70.7% and 3 dB in decibels units.

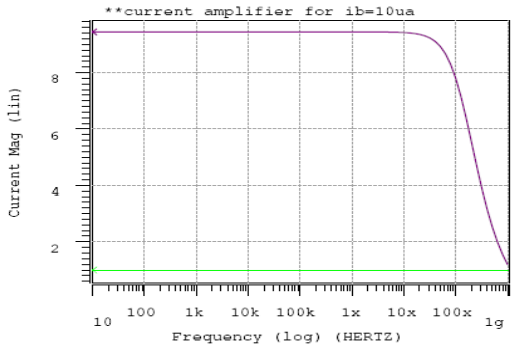


Fig 4.7 Frequency response for Current Amplifier

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